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INTELLIGENT CYCLIC ADC. PRINCIPLES OF FUNCTIONING, OPTIMISATION AND ANALYSIS[2]

The aim of the paper is a presentation of conceptual backgrounds of a new approach to design and analysis of high-efficient intelligent analog-to-digital converters (ADC). Particularities of intelligent conversion, methods of its practical implementation and advantages over conventional methods of conversion are discussed. The analysis is carried out on the example of "intelligent" cyclic ADC (IC ADC), which employ, as the prototype, the architecture of known cyclic ADC developed by Analog Devices Inc. [1, 2]. There is shown the method of extension of the proposed approach for development of more advanced versions of IC ADC with extended range of application and processing possibilities. The paper generalizes the results of previous investigations**.**

Keywords: cyclic ADC, intelligent conversion, optimisation, ENOB

1. INTRODUCTION

Cyclic A/D converters (CADC) belong to the class of iterative converters, which form the code of each sample of the input signal accumulating information delivered in previous cycles of conversion [1-3]. Quality of CADC work depends on entirety of utilisation of the resources of their components. This, in turn, depends on degree of utilisation, in the structure of CADC, of the prior information about input signals and noises, architecture and parameters of the analogue part, principle of the sample codes forming used in CADC, as well as of information delivered by the analogue part in sequential cycles of conversion.

Recently, no advanced mathematical tools exist enabling analytical investigation of the conversion quality that is conditioned by following reasons. First, the small -bit logic elements used for the codes forming in CADC makes the set of possible codes of the samples the discrete set, which consists of relatively small number of binary words. The second reason is multiple non-linearity of CADC analogue part. Both the reasons make impossible a search of the extremes of analytical criterions of conversion quality, as well as analysis of their dependencies on the parameters of analogue components and other factors influencing the CADC performance.

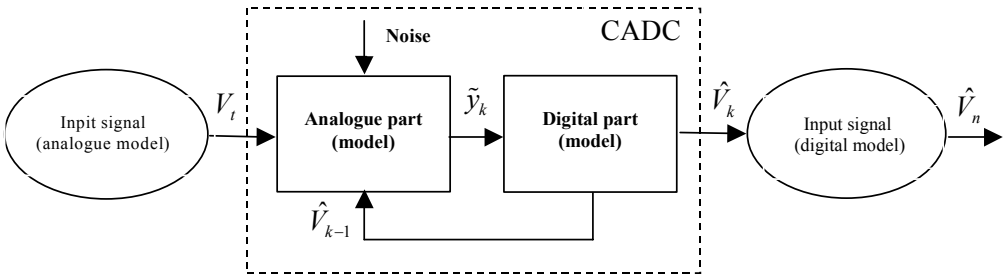

Fig. 1. Full model of the cyclic conversion process.

[1] On leave from Moscow Institute of Electronics and Mathematics, Chair of Cybernetics, Russia.

[2] The work was presented, in part, at the International Conference on Signals and Electronic Systems (ICSES'2006), Łódź, September 17-20, 2006 [23].

In the paper, backgrounds of the approach permitting to formulate analytical criterions of CADC quality using mathematical models of their analogue and digital parts, input signals and noises (see Fig. 1, and Sect. 3) are discussed. These criterions permit to investigate the dependence of CADC performance on the structure, characteristics and parameters of the analogue components, noises, input signals, as well as on the algorithm used for the codes forming. The results of analysis determine the close-to-optimal parameters of the main analogue elements and the algorithm of the digital part that, finally, determines the most appropriate structure and method of the converter realisation. Simultaneously, the proposed approach enables numerical evaluation of expected characteristics of conversion quality. Its application to CADC design enables realisation of the converters best in corresponding class of converters and applicable to conversion of wider classes of signals.

Presentation of the approach is carried out on the example of new "intelligent" CADC (IC ADC, see also works [4-13]). Nevertheless, it can be applied successfully to design of other classes of intelligent ADC employing iterative principle of the samples conversion: e.g. cascade (pipe-line) ADC [3], redundant signed digit (RSD) ADC [14] and others.

The paper consists of six sections. Sect. 2 is devoted to presentation of general principles of intelligent conversion and conditions enabling its practical implementation. In Sect. 3, main mathematical models used in CADC analysis are discussed. Sect. 4 presents the principles of IC ADC optimisation, and explains differences in functioning of IC ADC and conventional CADC. In Sect. 5, methods of IC ADC optimisation and perspectives of their development are discussed. Sect. 6 summarizes the results of the paper.

2. ROLE OF DIGITAL PART IN IMPROVEMENT OF CADC PERFORMANCE

Objective of IC ADC as the intelligent device is fastest and most adequate (accurate) restoring of digital model of the input signal acting during each moment of the signal conversion. Term "intelligent " CADC (IC ADC) reflects a series of particularities in the principles of conversion implemented in their construction. Namely, digital part of IC ADC is designed and operates in the way enabling realization of following, unfeasible in conventional CADC operations:

1. Adaptive constructing and correction of digital model of the input signal. IC ADC realise this task taking into account transformations of the signal in the analogue part, as well as influence of the noises and errors of the signal observation and processing. Prior models of the input signal and the analogue and digital parts of the converter can be known completely or partially depending on the construction and completeness of prior information.
2. The goal of IC ADC is the most accurate estimation of digital values of the signals acting at its input. The estimation (forming the code of the input signal or process values) is carried out using a full model of conversion process. This model is constructed taking into account (see Fig. 1 and Sect. 3):
   - all available prior information about the input signal, analogue part and digital parts functioning. This information is given in the form of corresponding models which should permit to consider the changes of IC ADC parameters caused by adaptive adjusting, as well as noises, errors and other factors influencing their performance;
   - information acquired and stored during conversion of the current and previous samples;
   - current measure of conversion quality permitting to correct and optimise the work of IC ADC in each cycle of conversion in the way ensuring the quickest and accurate restoring of the digital model of the signal.
3. Digital part of IC ADC forms adequate model of the signal acting at its input and predicts

its evolution. The predictions are used to form the signal of error, next used for adaptive adjustment of the analogue part of IC ADC. The adjusting is performed in the way maximally increasing the amount of information about the input signal delivered to digital part and, as result, increasing the quality and speed of conversion.

The discussed in the paper new approach to IC ADC design and analysis is based on the approach presented in works [12, 13]. The results of these works enable concurrent optimisation of the analogue and digital parts of mixed-signal adaptive estimation (measurement) systems that is done taking into account the prior information and data delivered by adaptively adjusted analogue part. Being applied to the cyclic converters, algorithms derived in [12, 13] permit to determine the structure and parameters of the analogue part and codes forming algorithm that ensures achievement of close to theoretically available quality of conversion. Simultaneously, this ensures practically full utilization of the resources of the analogue and digital elements of IC ADC that is optimises their construction.

However, results of works [12, 13] cannot be used for IC ADC design directly and require radical changes in the structure and principles of their digital parts functioning. The reason is impossibility to realise new principles of conversion in the frame of known CADC with low-bit logic in the digital parts. The reason is a small number of elements in discrete sets $\Omega^{(\hat{V})}$ of possible values of the codes $\hat{V}_k$ - the models of input signal formed by CADC in each cycle (see also Sect. 4). Narrow set $\Omega^{(\hat{V})}$ of these models cannot reflect adequately the much more numerous set $\Omega^{(V)}$ of the continuous mathematical models of the input signals. The latter crucially restricts possibilities to "intellectualize" these converters. Also, mixed signals - continuous ones in the analogue part and discrete ones in the digital part of CADC - do not permit to investigate and optimise the converters using known analytical tools. These problems can be solved by the transition from low-bit logic to long-bit arithmetic in computing of the input signal codes (the length of binary words $N_{comp} = 16, 24, 32$ bit depending on required resolution of converter). This transition creates following, qualitatively new possibilities for CADC design.

First of all, it radically extends (to $2^{N_{comp}}$ elements) the set $\Omega^{(\hat{V})}$ of possible codes $\hat{V}_k$ values, $k = 1, \ldots, n$, that permits to consider this set as practically infinite (continuous) set. The latter permits to refer each long binary word $\hat{V}_k$ to corresponding analogue value V from the set $\Omega^{(V)}$ of possible input signals. As result, the sets $\Omega^{(\hat{V})}$ and $\Omega^{(V)}$ of the signals and codes can be considered as equivalent sets (errors caused by transition from decimal to binary presentation and back are of $2^{-N_{comp}} << 1$ order). This enables adequate and mathematically uniform description of processes in analogue and digital parts of IC ADC using continuous variables, models and known methods of theoretical analysis. Full mathematical model of conversion process (see Fig. 1) permits to formulate the analytical criterion of conversion quality, which takes into account all significant factors influencing the quality of conversion. Optimal codes computing algorithm are the algorithms, which provides maximum, in each cycle, quality of conversion. Solution of optimisation task can be carried out by known methods of optimal estimation theory.

Secondly, transition to long-bit codes presentation and computing is necessary conditions for "intellectualisation" of CADC in the sense of the given above definitions. Corresponding converters acquires possibility to restore and correct the continuous model of input signal and use it for optimisation of the work of data acquisition and processing units.

Another important result of the transition to long-bit codes computing is thoroughly verified high numerical closeness of analytical results and results of simulation experiments carried out using full mathematical models of IC ADC. This makes simulations an important

tool for the fast and accurate IC ADC analysis. In particular, in many cases, they may replace complex analytical calculations. Moreover, they enable the obtaining the accurate results in situations, where analytical solutions are too complex or impossible.

One should notice that the long-bit units in digital parts of IC ADC, at least in less advanced versions of the converters [4-12, 15], have simple structure and can be realized without significant increase of the size, cost and energy consumption in comparison with their conventional prototypes. Moreover, the digital part can be completely excluded from the architecture of IC ADC, if its analogue part is realized as an independent analogue element connected to the microprocessor employing it as the analogue input [11, 15]. In that case, functions of the digital part can be realized by corresponding service program of microprocessor. The latter prompts the most efficient method of IC ADC utilization by integrating its analogue part with microprocessor.

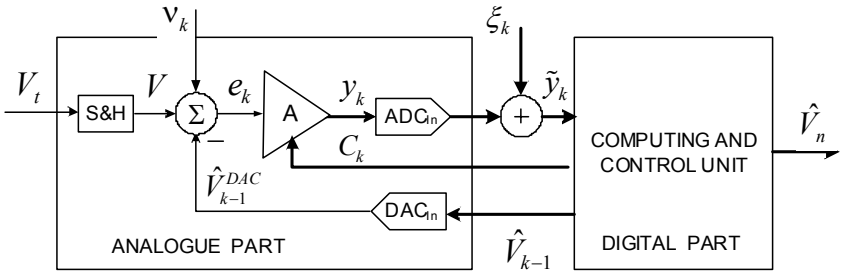

Fig. 2. General structure of intelligent sub-optimal IC ADC [1].

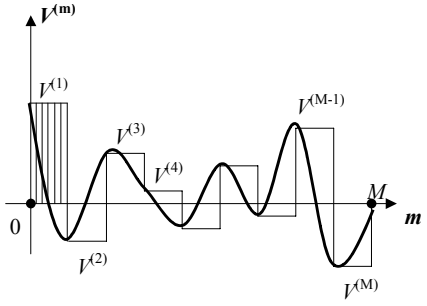

Fig. 3. Input signal after sampling in S&H unit.

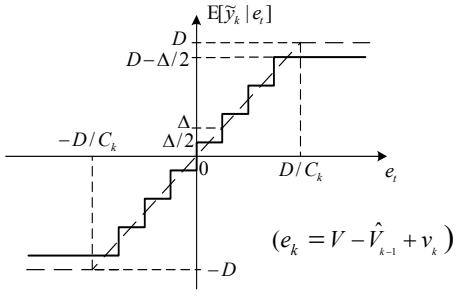

Fig. 4. Transition function of the analogue part.

3. MATHEMATICAL MODELS

In this section, mathematical models enabling formal description of CADC and IC ADC work are discussed. General architecture of CADC is presented in Fig. 2, where V_t (see also

Fig. 1) is the signal at the converter input. Values $\hat{V}_k$, ($k = 1, \ldots, n$) are intermediate binary codes (estimates) of the currently converted sample V. Value $\hat{V}_n$ is the final code of the sample V. Analogue part of IC ADC has the same structure as the cyclic converters AD678, AD1678 [1], and was used as a basic for sub-optimal IC ADC considered in [4-12] and in this paper. CADC of other classes employ similar general principle of conversion. Differences in constructions do not hinder their modification into intelligent CADC in the way similar to the described in the paper.

Full mathematical model of the conversion process includes the model of signal, and of the analogue and digital parts. The simplest and, in many cases, sufficiently adequate mathematical model of the input signal is Gaussian process with zero spectral power density outside the frequency band [$-F$, F]. Than, the signal V_t can be presented as a sequence of samples $V^{(m)} = V(mT)$, in general case correlated (see Fig. 3, $m = 1, \ldots, M$, $T = 1/2F$). CADC realize the conversion of each sample $V^{(m)}$ in $n = T/\Delta t_0$ cycles, where $\Delta t_0 = 1/F_0$ is the duration of the single conversion cycle.

Model of the analogue part consists of a number of mutually connected models of particular elements. Samples $V^{(m)} = V$ (index m is further omitted) are formed in the sample-and-hold block (S&H in Fig. 2), which holds the analogue signal V at the first input of subtracting unit Σ during the interval T. In each k-th cycle of conversion, signal at the subtractor Σ output (at the amplifier A input) has the form:

$$e_k = V - \hat{V}_{k-1}^{DAC} + \nu_k = V - \hat{V}_{k-1} + \zeta_k , \qquad (1)$$

which can be considered as the mathematical model of the work of the "S&H and Σ" unit.

Value $\hat{V}_{k-1}^{DAC} = \hat{V}_{k-1} - \Delta\hat{V}_{k-1}^{DAC}$ in (1) represents the analogue equivalent of the estimate $\hat{V}_{k-1}$ formed in the digital part of CADC in previous cycle and converted by the feedback D/A converter $\mathrm{DAC_{In}}$. Errors of "rounding" caused by the finite resolution of (ideal) D/A converter are equal to zero: $\Delta\hat{V}_{k-1}^{DAC} = 0$, if its resolution N_{DAC} is greater than the length $N_{k-1}$of the binary word $\hat{V}_{k-1}$, and $\Delta\hat{V}_{k-1}^{DAC} \neq 0$ in opposite case (values $\hat{V}_{k-1}$ are truncated after N_{k-1}-th bit). Errors caused by non-ideality of actual $\mathrm{DAC_{In}}$ should be considered additionally. Variable $\zeta_k = \nu_k + \Delta\hat{V}_{k-1}^{DAC}$ represents the summary noisy component acting at the amplifier (A) input. Value ν_k is a sum of the analogue noises and errors in the feedback chain, S&H and Σ units, as well as possible external noises.

Coarse low-bit pre-converter $\mathrm{ADC_{In}}$ at the output of CADC analogue part converts the amplified analogue signal $y_k = C_k e_k$ into the N_{ADC}-bit binary code ("observation") $\tilde{y}_k$. Resolution of $\mathrm{ADC_{In}}$ may have values $N_{ADC} = 1 \div 6$ bits depending on the construction of CADC. Static transition function of the unit "Amplifier and $\mathrm{ADC_{In}}$" has step-wise form (see Fig. 4). The always finite input range [$-D$, D] of pre-converter $\mathrm{ADC_{In}}$ is assumed to be the only source of possible saturation of the analogue part. In our works [4-12], following, simple but sufficient for the analysis approximate mathematical model of the unit "Amplifier and $\mathrm{ADC_{In}}$" is used:

$$\tilde{y}_k = \begin{cases} C_k e_k + \xi_k & \text{for} \quad C_k \,|\, e_k \,| \leq D \\ D sign(e_k) + \xi_k & \text{for} \quad C_k \,|\, e_k \,| > D . \end{cases} \qquad (2)$$

Here, ξ_k is the quantization noise introduced instead of strict description of distortions caused by the step-wise non-linearity of the analogue part. In initial researches in majority of our works, power of quantisation noise σ_ξ^2 was assessed using the commonly used in ADC analysis approximate Widrow–Bennet's formula [16-18]:

$$\sigma_\xi^2 = \frac{\Delta_{ADC}^2}{12} = \frac{D^2}{3} 2^{-2N_{ADC}} . \tag{3}$$

This relationship is valid under assumption that quantization noise ξ_k has uniform distribution inside of the quantization interval $[-\Delta/2, \Delta/2] = [-D/2^{N_{ADC}}, D/2^{N_{ADC}}]$). Further investigations shown that for the cyclic ADC and IC ADC this assumption is not true and Eq. (3) should be corrected [5, 10-12]. Equations (1), (2) determine full static mathematical model of the analogue part of IC ADC. It can be generalized in the way allowing the analysis of the transition effects. However, complexity of the task dictates first the investigation of particularities of IC ADC functioning at the static level.

Mathematical model of the digital part of CADC can be introduced taking into account common for each CADC iterative methods of the codes forming. For each $k = 1, \ldots, n$, CADC builds the intermediate estimate $\hat{V}_k$ of the currently converted sample V by adding the respectively transformed observation $\tilde{y}_k$ to the estimate $\hat{V}_{k-1}$ formed in previous cycle:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k ; \quad (k = 1, \ldots, n) \tag{4}$$

One can show [19] that for $N_{k-1} > N_{DAC}$ adding the correction term $L_k C_k \Delta\hat{V}_{k-1}^{DAC}$ in the right side of (1) compensates the influence of truncation errors $\Delta\hat{V}_{k-1}^{DAC}$ appearing in the signal $e_k = V - \hat{V}_{k-1}^{DAC} + v_k$ formed at the amplifier (A) input. Further, we assume this correction is done and perform the analysis using, without loss of accuracy, following expression for the residuals: $e_k = V - \hat{V}_{k-1} + v_k$ (without the term $\Delta\hat{V}_{k-1}^{DAC}$).

Each new estimate $\hat{V}_k$ formed by the digital part of CADC is stored during one cycle in the memory unit of CADC. Values of coefficients L_k depend on the construction of converters, and on the gains C_k (see Sect. 4). Initial estimate $\hat{V}_0 = V_0$ is determined by mean value V_0 of the input signal. Sequences of final codes $\hat{V}_n$ represent the digital model of realization of the input signal, and can be routed to the external addressee of controlling unit. Model (4) is universal and can be used for description of the codes forming in each iterative ADC.

4. DIFFERENCES BETWEEN KNOWN AND INTELLIGENT CADC FUNCTIONING

The design of known CADC does not employ the prior information about the input signals V_t. In turn, IC ADC are designed taking into account always random nature of the input signals, and one of its objectives is optimal utilization of the prior information about distribution of the signal values (Bayesian approach). In our researches, we assume that the input signals are Gaussian zero-mean processes with the power not greater than σ_0^2 in frequency band of the signals $[-F, F]$. At the current stage of investigations, we assume that

each next sample is converted independently. The latter permits to reduce the analysis of IC ADC work to analysis of the processes during conversion of a single sample. One should notice that such approach is common in ADC design. It is worth to notice that this assumption means that correlations between the samples are not considered.

As it was said above, main difference between the conventional and intelligent CADC concerns the principles of realisation and functioning of their digital parts. For this reason, main attention is to be paid to the analysis of these differences and of the effects caused by them. In known CADC [1-3], each intermediate code $\hat{V}_k$ is formed by adding the properly shifted N_{ADC}-bit observation $\tilde{y}_k$ to previous estimate $\hat{V}_{k-1}$ stored in the memory unit of the digital part. New estimate $\hat{V}_k$ replaces the previous estimate $\hat{V}_{k-1}$ in the memory unit and, simultaneously, is routed to the input of the N_{DAC}-bit feedback D/A converter $\mathrm{DAC}_{\mathrm{In}}$. Resolution N_{DAC} of $\mathrm{DAC}_{\mathrm{In}}$ is always not smaller than length N_k of the codes $\hat{V}_k$. Analogue equivalent $\hat{V}_k^{DAC}$ of the digital estimate $\hat{V}_k$, ($\hat{V}_k^{DAC} = \hat{V}_k$) is routed to the second input of the subtractor Σ, which forms new residual $e_{k+1} = V - \hat{V}_k + \nu_{k+1}$. Signal e_{k+1} is routed to the amplifier A and, after amplification, to the input of $\mathrm{ADC}_{\mathrm{In}}$, and $(k+1)$-th cycle of sample code forming begins.

This process is terminated when the final estimate $\hat{V}_n$ reaches maximal achievable accuracy. In general case, this moment depends on the feedback $\mathrm{DAC}_{\mathrm{In}}$ resolution, quality of the S&H unit and the power of analogue noises acting at the input of amplifier. It is shown [12,13] that numerical assessment of the moment n^* of termination of resolution growth – "threshold number of cycles" - can be obtained from the equation:

$$P_{n^*} = E[(V - \hat{V}_{n^*})^2] = \sigma_\nu^2. \tag{5}$$

where σ_ν^2 is the summary mean power of errors and noises at the amplifier input. Values $P_k = E[(V - \hat{V}_k)^2]$ describe the mean square error (MSE) of conversion errors after k cycles of conversion (in (5), $k = n*$).

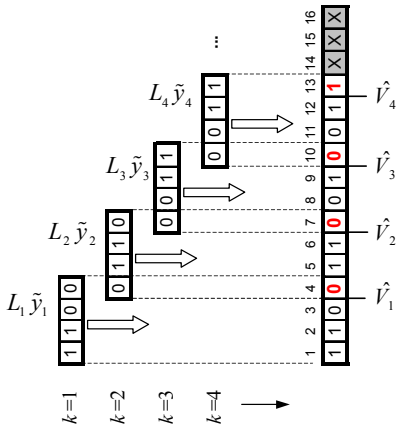

Fig. 5. Code forming in conventional CADC.

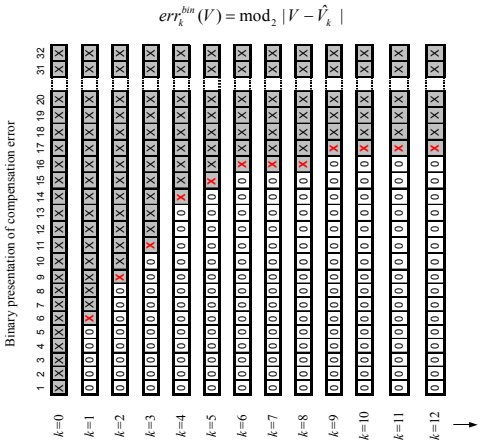

Fig. 6. Code computing in IC ADC.

In known CADCs, prior information about noise in the analogue part is used only for evaluation of the number $N_{ADC} - m_k$ of significant bits in each observation $\tilde{y}_k$. The number m_k of "questionable" bits is defined heuristically (empirically) taking into account the possibility of errors in these bits. In each new cycle, the code $\hat{V}_{k-1}$ is supplemented by $N_{ADC} - m_k$ bits of observation $\tilde{y}_k$ with overlapping of m_k least significant bits (LSB) of the code $\hat{V}_{k-1}$ and m_k most significant bits (MSB) of properly shifted N_{ADC}-bit code $\tilde{y}_k$ (see Fig. 5). For this to be possible, the code $\tilde{y}_k$ should be shifted, in each cycle, by $N_{k-1} = \Sigma_{i=1}^{k-1}(N_{ADC} - m_i)$ positions up ($k = 1, \ldots, n$; $N_0 = 0$, $m_k = 1 \div 3$ bit).

The number N_{k-1} of positions by which observations $\tilde{y}_k$ are shifted determines the gains L_k in recursion (4). Considering this recursion as the equation for decimal values, which respond to corresponding binary codes, the gains L_k can be written in the form of integer powers of two:

$$L_k = L_1 2^{-N_{k-1}} = L_1 2^{-\Sigma_{i=1}^{k-1}(N_{ADC} - m_i)} \tag{6}$$

The initial value of L_1 in (6) is determined by the initial value of the gain C_1.

For each $k = 1, \ldots, n$, unit Σ subtracts the analogue value $\hat{V}_{k-1}^{DAC}$ from the sample V held at the S&H unit output. Assuming that the converter $\mathrm{DAC_{In}}$ is ideal, one may notice that for the remaining group of $N_{DAC} - N_{k-1}$ MSB of the analogue signal $e_k = V - \hat{V}_{k-1}^{DAC} + \nu_k$ could be properly converted, shifted and added to the estimate $\hat{V}_{k-1}$, and values e_k should be amplified, in each cycle, exactly by

$$C_k = L_k^{-1} = C_1 2^{\Sigma_{i=1}^{k-1}(N_{ADC} - m_i)} \tag{7}$$

times. The initial value of the gain $C_1 = FSR/2D$ depends on the ratio of input full-scale range (FSR) of CADC and input range [$-D$, D] of pre-converter $\mathrm{ADC_{In}}$. Any deviation from this relationship increases the probability of errors in upper bits of the code $\hat{V}_k$ (see below).

Contrary to the known CADCs, in a IC ADC each code $\hat{V}_k$ and digital gain L_k are the long-bit binary words always of the constant length N_{comp}. Each new estimate $\hat{V}_k$ is computed according to recursion (4). However, the values $L_k\tilde{y}_k$ are not shifted observation but N_{comp}-bit products of corresponding N_{comp} and N_{ADC} binary words. Each new N_{comp}-bit code $\hat{V}_k$ contains on the average a greater number of significant bits than the previous code $\hat{V}_{k-1}$. This process is illustrated in Fig. 6, where changes of the binary code of conversion error $err_k^{bin}(V) = \mathrm{mod}_2 |V - \hat{V}_k|$ in sequential cycles are presented. Positions of zeros in Fig. 6 correspond to the numbers of significant, non-erroneous bits in intermediate codes $\hat{V}_k$.

As it was said in Sect. 1, application of the long-bit-word arithmetic in IC ADC digital part enables consideration of the set $\Omega^{(\hat{V})}$ of the of codes as the continuous set that removes constraint (6). For this reason, set $\Omega_k^{(L)}$ of possible values L_k in the recursion (4) can be considered as the continuous set (with errors not greater than of $\Delta_{comp} = 2^{-N_{comp}}$ order, on a decimal scale). The latter removes constraint (7) on the sets $\Omega_k^{(C)}$ of permissible values of the analogue gains C_k although the reversed dependence $C_k \sim L_k^{-1}$ remains valid also for IC ADCs. Removal of these constraints permits to set the gains C_k to the values greater than corresponding values in conventional CADCs. In turn, greater gains C_k increase, in each cycle, the signal to quantisation noise ratio at the at the $\mathrm{ADC_{In}}$ output which is defined by the formula:

$$SNR_k^{ADC} = \frac{E[(C_k e_k)^2]}{\sigma_\xi^2}, \tag{8}$$

that increases, in each cycle, the mean number of correct bits or "efficient number of bits" - ENOB [16] in the codes $\hat{V}_k$. However, enlargement of gains C_k is limited by the necessity to exclude, in each cycle of conversion, the probability P^{sat} of overloading the IC ADC which causes an appearance of distorted codes at its output.

The random character of the signals at CADC input and randomisation of residual signals e_k caused by noise and multiple summation of random residual signals preserves in each cycle a definite probability of overloading the converter. The impossibility to exclude random effects and the necessity to exclude overloading makes the introduction of the probabilistic guarantees of elimination of CADC overloading necessary. This can be done in the form of a requirement to the probability of CADC saturation which should not exceed, for each $k = 1, \ldots, n$, the given confidence level $(1 - \mu)^n$. Mathematically this requirement (condition of statistically fitted observation [12, 13]) can be formulated as follows:

$$\Pr^{sat} = \Pr\left(|e_k| > \frac{D}{C_k} \;\middle|\; \tilde{y}_1^{k-1} \right) = 1 - \int_{\hat{V}_{k-1} - D/C_k}^{\hat{V}_{k-1} + D/C_k} p(V \mid \tilde{y}_1^{k-1}) \mathrm{d}V < \mu, \tag{9}$$

where $p(V \mid \tilde{y}_1^{k-1})$ is the posterior distribution of the input signal values after k-1 cycles of conversion, and $\tilde{y}_1^{k-1} = (\tilde{y}_1, ..., \tilde{y}_{k-1})$ is the sequence of observations obtained in k-1 cycles.

Equation (9) determines, for each $k = 1, \ldots, n$, the continuous set Ω_{Ck} of permissible gains C_k which exclude rough errors in corresponding codes $\hat{V}_k$ at the confidence level μ. Value μ

determines the acceptable probability of saturation for the considered class of converters (confidence level). In practice, numerical values μ may lay in the interval $10^{-3} \le \mu \le 10^{-9}$. Let us notice that according to IEEE Standard 1241 [16, p.4.13], the value $(1-\mu)^n$ represents the acceptable word error rate (WER) of conversion.

Application of the long-word arithmetic and the possibility to consider $\hat{V}_k$, L_k, C_k and $L_k\tilde{y}_k$ as *continuous* variables, permit to construct, using models (1), (2), the continuous model of the converter which can be optimised using the known methods and mathematical apparatus of optimal estimation theory. The most efficient approach to IC ADC optimisation is the application of optimal "intelligent" algorithms [12, 13], which cannot be applied to the conventional CADC with discrete logic.

It is necessary to notice that non-linearity of the analogue part of each CADC makes, in initial cycles, the distribution of quantisation noise ξ_k strongly non-Gaussian even for Gaussian signals at their input. This significantly complicates the optimisation of the converters. Nevertheless, the discussed analytical approach simplifies and put in order the search for sub-optimal algorithms of code computing which ensure maximal conversion quality.

5. METHODS OF OPTIMISATION AND PERSPECTIVES OF IC ADC DESIGN

In the simplest versions of IC ADC considered in [4-12], the conversion algorithm has the form presented by relationships (2), (4) where both the sets Ω_V and $\Omega_{\hat{V}}$ of possible values of the signals V and codes $\hat{V}_k$ are continuous and equivalent. Then, the optimisation of the algorithm can be reduced to definition of the values L_k and C_k minimizing the mean square error (MSE) of conversion:

$$P_k = E[(V-\hat{V}_k)^2] = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}[V-\hat{V}_k(\tilde{y}_1^k)]^2\, p(V \mid \tilde{y}_1^k)\, p(\tilde{y}_1^k)\, dV\, d\tilde{y}_1^k , \qquad (10)$$

under additional constraint (9). This task can be formulated in an equivalent form, but more convenient for IC ADC analysis form using, as the criterion of conversion quality the effective number of bits (ENOB) connected with MSE by a monotonic logarithmic dependence [12, 20-22]:

$$N_k = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_k}\right)\text{[bit]}. \qquad (11)$$

Value σ_0^2 in (11) is the maximal permissible mean power for the given converter of input signals, and $P_1 = \sigma_1^2 \le \sigma_0^2$. It is worth to notice that Eq. (11) represents the amount of Shannon's information [12, 21, p.3.3] about the Gaussian input signal V delivered by the sequence of observations $\tilde{y}_1^k = (\tilde{y}_1, ..., \tilde{y}_k)$.

Below, a more advanced form of the conversion algorithm is considered which generalises the algorithm considered in [4-12] and improves the characteristics of the IC ADC. This algorithm is based on the algorithm derived in [13] and allows the structure analysis and identification (parameters estimation) of complex input signals.

We assume also that signals at the subtractor Σ input have a structure of the sum of J signals $x_k^{(r)}$, ($r = 1, \ldots, J$, $k = 1, \ldots, n$) of known form, but unknown random amplitudes $\theta^{(J)}$:

$$V_k = \sum_{r=1}^{J} \theta^{(r)} x_k^{(r)} = \boldsymbol{\theta}^T \boldsymbol{x}_k , \tag{12}$$

where $\boldsymbol{x}_k = (x_k^{(1)}, ..., x_k^{(J)})^T$ and $\boldsymbol{\theta} = (\theta^{(1)}, ..., \theta^{(J)})^T$ are the column vectors.

In the Gaussian case, the optimal algorithm ensuring minimization of MSE and ENOB of estimates $\hat{V}_k$ has the form [13]:

$$\hat{V}_k = \hat{\boldsymbol{\theta}}_k^T \boldsymbol{x}_k ; \quad \hat{\boldsymbol{\theta}}_k = \hat{\boldsymbol{\theta}}_{k-1} + \boldsymbol{L}_k \tilde{y}_k , \tag{13}$$

$$\boldsymbol{L}_k = \frac{C_k \boldsymbol{P}_k \boldsymbol{x}_k}{\sigma_\xi^2 + C_k^2 \sigma_\nu^2} = C_k^{-1} \left[\boldsymbol{I} - \boldsymbol{P}_k \boldsymbol{P}_{k-1}^{-1} \right] \boldsymbol{x}_k ; \quad C_k = \frac{D}{\alpha \sqrt{\sigma_\nu^2 + \boldsymbol{x}_k^T \boldsymbol{P}_{k-1} \boldsymbol{x}_k}} ; \tag{14}$$

$$\boldsymbol{P}_k = \boldsymbol{P}_{k-1} - \frac{C_k^2 \boldsymbol{P}_{k-1} \boldsymbol{x}_k \boldsymbol{x}_k^T \boldsymbol{P}_{k-1}}{\sigma_\xi^2 + C_k^2 (\sigma_\nu^2 + \boldsymbol{x}_k^T \boldsymbol{P}_{k-1} \boldsymbol{x}_k)} , \tag{15}$$

where $\boldsymbol{P}_k = E[(\boldsymbol{\theta} - \hat{\boldsymbol{\theta}}_k)(\boldsymbol{\theta} - \hat{\boldsymbol{\theta}}_k)^T]$ is the $(J \times J)$ covariance matrix of estimation errors, and $\boldsymbol{I}$ is $(J \times J)$ diagonal unity matrix. Initial conditions for (13)-(15) are determined by the mean values $\boldsymbol{\theta}_0 = (\theta_0^{(1)}, ..., \theta_0^{(J)})^T$ and covariance matrix $\boldsymbol{P}_0 = E[(\boldsymbol{\theta} - \boldsymbol{\theta}_0)(\boldsymbol{\theta} - \boldsymbol{\theta}_0)^T]$ of the prior distribution of amplitudes $\boldsymbol{\theta}$.

Parameter α in the expression for the analogue gain C_k in (14) is a saturation factor, which guarantees the elimination of overloading of the analogue part at the confidence level μ (see Eq. (9)). In the Gaussian case, its value satisfies the equation [12, 13]:

$$\Phi(\alpha) = \frac{1}{\sqrt{2\pi}} \int_0^{\alpha} \exp\left\{ -\frac{x^2}{2} \right\} dx = \frac{1 - \mu}{2} . \tag{16}$$

Equations (13)-(15) describe the work of digital and analogue part of sub-optimal IC ADC and enable close –to-optimal restoring the digital model of input signal (12). The model of the analogue part has the same structure as in IC ADC considered in [4-12]. One may check that in the scalar case ($\boldsymbol{\theta} = V$, $\boldsymbol{x}_k = 1$) the latter formulas take the form of scalar algorithm used for optimisation of IC ADCs in [4-12]:

$$L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_\nu^2} = C_k^{-1} \left(1 - \frac{P_k}{P_{k-1}} \right); \quad C_k = \frac{D}{\alpha \sqrt{\sigma_\nu^2 + P_{k-1}}}, \tag{17}$$

$$P_k = \frac{\sigma_\xi^2 + C_k^2 \sigma_\nu^2}{\sigma_\xi^2 + C_k^2 (\sigma_\nu^2 + P_{k-1})} P_{k-1} \tag{18}$$

(formulas (2), (4) remain unchanged).

The extended algorithm (2), (4), (13)-(15), permits to design more advanced versions of IC ADC than these analysed in [4-12]. For instance, assumption $\boldsymbol{x}_k = (1, k)$ and $\boldsymbol{\theta} = (V, \gamma)$ transforms relationships (13)-(15) into extended algorithm, which may realise, apart of the estimation of useful component V, approximate evaluation and correction of the slew rate of S&H unit. Using (2),(4),(13)-(15), one can realise IC ADCs based on estimation of the Fourier transform of the input signals. In this case, one should take $x_k^{(r,1)} = \sin[2\pi(r-1)k/J]$ and $x_k^{(r,2)} = \cos[2\pi(r-1)k/J]$ that makes model (12) a truncated Fourier series of the input signal. Than, extended algorithm (2), (4), (13)-(15) converts the input signal after initial the estimation of the truncated Fourier spectrum, and codes $(\hat{V}_1, ..., \hat{V}_n)$ are computed using formula $\hat{V}_k = \hat{\boldsymbol{\theta}}_k^T \boldsymbol{x}_k$. Final code of the sample $\hat{V}_n = \hat{\boldsymbol{\theta}}_n^T \boldsymbol{x}_n$ is determined by the final vector-estimate $\hat{\boldsymbol{\theta}}_n$ of Fourier coefficients. Thus, realised in this way IC ADC gives, apart of the codes of the signal, its spectral characteristics.

Systems built according to (2), (4), (13)-(15) preserve a most important (for applications) property of estimations systems and converters built according to (2), (4), (17), (18) – extremely (exponentially) fast diminution of MSE of estimates $\hat{V}_k$ at the initial "pre-threshold" interval $1 \le k \le n^*$ (see also [13]):

$$P_k = E[(V - \hat{V}_k)^2] = \boldsymbol{x}_k^T \boldsymbol{P}_k \boldsymbol{x}_k = \tag{19}$$

$$= \boldsymbol{x}_k^T \boldsymbol{P}_{k-1} \boldsymbol{x}_k \cdot \frac{(\sigma_\xi^2 + C_k^2 \sigma_\nu^2)}{\sigma_\xi^2 + C_k^2 (\sigma_\nu^2 + \boldsymbol{x}_k^T \boldsymbol{P}_{k-1} \boldsymbol{x}_k)} = P_{k-1}(1+Q^2)^{-1} = \sigma_0^2 (1+Q^2)^{-k},$$

where

$$Q^2 = \frac{W_{sign}}{W_{noise}} = \frac{C_k^2 E(e_k^2)}{\sigma_\xi^2} = \left(\frac{D}{\alpha \sigma_\xi} \right)^2 = \frac{3}{\alpha^2} 2^{2N_{ADC}} = SNR_k^{ADC} \tag{20}$$

is the SNR at theoutput of the analogue part (ADC_{In}). The right side of (19) is obtained under assumption that the changes of the vector-process $\boldsymbol{x}_k$ during one-cycle estimation are negligibly small. For $k > n^*$, the rate of MSE diminution is much slower than in the initial interval of estimation (depends on k hyperbolically). The threshold number n^* can be evaluated using (5) and the right side of Eq. (19), which permit to obtain the relationship [12, 13]:

$$n^* = \frac{1}{\log_2(1+Q^2)} \log_2 \left(\frac{\sigma_0^2}{\sigma_\nu^2} \right). \tag{21}$$

This formula determines the optimal number of cycles of processing of the input signal. For $k > n^*$, noise ξ_k is practically suppressed, adaptive adjustment of the analogue part does not improve the estimates and can be stopped [12]. Further, slow growth of the accuracy of estimates $\hat{V}_k$ is maintained by digital processing the observations $\tilde{y}_k$.

Values of the gains (14), (17) are optimal only in the Gaussian case and, as it was noticed in Sect. 4, become sub-optimal in non-linear IC ADCs due to non-Gaussian distribution of quantization noise ξ_k. For this reason, the algorithms presented above can be corrected in a

way improving additionally the quality of conversion (see [6, 9, 19] also below). It is worth to notice (see also [10,18]) that, independently from the form and distribution of the input signals, beginning with the threshold cycle (for $k \geq n^*$) the distribution of conversion errors takes the Gaussian form, and its values lie, with the probability close to the confidence level 1-μ inside the intervals $[-\alpha\sqrt{P_k}\,;\,\alpha\sqrt{P_k}\,]$. This permits to use Eq. (11) as an adequate analytical evaluation of ENOB of IC ADC at threshold (and next) cycles of conversion.

Methods of algorithm (2), (4), (17), (18) correction were investigated in two directions. Main attention was paid to the definition of maximal permissible, sub-optimal values of the gains $C_1^{\max},...,C_n^{\max}$. The second direction was a correction of Eq. (3), which gives erroneous assessment of σ_ξ^2 values for low- bit $\mathrm{ADC_{In}}$.

According to [12, 13] (see also the left side of Eq. (20)), the greater gains C_k increases the SNR at the output of the analogue part and improve the accuracy of estimates $\hat{V}_k$. Therefore, the suboptimal values $C_k^{\max}$ can be determined as the maximal gains, which do not cause appearance of the IC ADC overloading (do not violate condition (9)) that determines the procedure of their search. As it was shown in [12, 13], in the Gaussian case the values of $C_k^{\max}$ do not depend on the values of the gains $L_1,...,L_n$. Simulation experiments confirmed a weak dependence of $C_k^{\max}$ values from the choice of gains L_k (if they do not cause divergence of the algorithm). For this reason, search of the sub-optimal values $C_k^{\max}$ was carried out under the gains L_k set to the values $L_k = C_k^{-1}$ or to the nominal values (17). Optimal values $L_k^{\min}$ were determined after definition of the values $C_k^{\max}$.

Different methods of practical definition of the most appropriate values $C_k^{\max}$, $L_k^{\min}$ were studied. The simplest way is a direct evaluation of the most appropriate values of the gains C_k in simulation experiments and computation of $L_k^{\min}$ according to the formula $L_k = C_k^{-1}$ for $k \leq n^*$, and formula (17) for $k > n^*$. The experiments were carried for the input signals - sequences of digital Gaussian samples distributed with the zero mean and standard deviation $\sigma_0 = FSR/2\alpha$. Special program registered the moments of the inequality $|e_k| \leq D/C_k$ violation in the series of $M = 10000$ samples. In each sequential cycle, gain C_k (initially set to the value (17)) was slowly increased until the moment of first violation of this inequality. Corresponding value $C_k^{\max}$ was registered and used as the sub-optimal gain for definition of the next sub-optimal value $C_{k+1}^{\max}$, which was determined in the same way. After definition of the sequence $C_1^{\max},...,C_n^{\max}$, the procedure was repeated for definition of sub-optimal sequence of the gains $L_1^{\min},...,L_n^{\min}$. The shortages of the method are relatively large time-consumption and lack of analytical support.

Another method of $C_k^{\max}$ definition, which permits to make their analytical assessments, is the "minimax" approach proposed in [9]. Its main idea consists in a setting the gains C_k to the maximal permissible values under least favourable values of the signal at the pre-converter $\mathrm{ADC_{In}}$ input. To derive the relationships for $C_k^{\max}$, following formula is to be used:

$$e_{k+1} = \left[1 - L_k C_k\right] e_k + L_k \xi_k + \nu_{k+1} - \nu_k = \frac{P_k}{P_{k-1}} \left(e_k - \frac{\xi_k}{C_k} \right) + \frac{\xi_k}{C_k} + \nu_{k+1} - \nu_k \approx$$
$$\approx \frac{\xi_k}{C_k} + \nu_{k+1} - \nu_k \qquad (22)$$

which can be easily derived from (2), (4), (17) under the assumption $\sigma_0^2 >> \sigma_\nu^2$ (the latter inequality leads to the inequalities $Q^2 >> 1$, $P_k / P_{k-1} \approx 1$ and, as result, to the equality $L_k C_k = 1 + O(Q^{-2})$). Taking into account the always-valid inequalities $|\xi_k| \le \Delta_{ADC} / 2 = D / 2^{N_{ADC}}$ and $|\nu_k| \le \Delta_\nu / 2$, one can obtain the relationship:

$$|e_{k+1}| \le e_{k+1}^{\max} = \frac{\Delta_{ADC}}{2C_k} + \Delta_\nu . \qquad (23)$$

Value $e_{k+1}^{\max}$ in (23) determines maximal changes of residual signal, which does not cause overloading of ADC_{In} and can be treated as the least favourable signal at the amplifier input. In turn, maximal gains $C_k^{\max}$ guaranteeing elimination of ADC_{In} overloading for any other signals $|e_{k+1}| \le e_{k+1}^{\max}$ satisfy the formula $C_{k+1}^{\max} = D / e_{k+1}^{\max}$. Substituting here Eq. (23) and assuming every previous gain $C_1^{\max}, ..., C_{k-1}^{\max}$ is sub-optimal, one may obtain the equation:

$$\frac{1}{C_{k+1}^{\max}} = \frac{e_{k+1}^{\max}}{D} = \frac{\Delta_{ADC}}{2D} \frac{1}{C_k^{\max}} + \frac{\Delta_\nu}{D} = \frac{\Delta_{ADC}}{2D} \left(\frac{1}{C_k^{\max}} - \frac{1}{C_\infty^{\max}} \right) + \frac{1}{C_\infty^{\max}} , \qquad (24)$$

which gives the approximate formula for the sub-optimal values $C_k^{\max}$ [23]:

$$C_{k+1}^{\max} = \frac{C_\infty^{\max}}{1 + \left(\frac{\Delta_{ADC}}{2D} \right)^k \left(\frac{C_\infty^{\max}}{C_1^{\max}} - 1 \right)} = \frac{C_\infty^{\max}}{1 + 2^{-kN_{ADC}} \left(\frac{C_\infty^{\max}}{C_1^{\max}} - 1 \right)} \qquad * \quad (25)$$

Values $C_1^{\max} = D / \alpha \sigma_0 = 2D / FSR$ and $C_\infty^{\max} = \left(2D - \Delta_{ADC}\right) / 2\Delta_\nu$ are the initial and final values of the gain $C_k^{\max}$, respectively; $FSR = 2\alpha \sigma_0$ denotes the full scale input range of IC ADC.

Equation (25) is highly sensitive to the analogue noise ν_k intensity of Δ_ν, and its accurate evaluation is independent and rather complex task. In practical design of IC ADC, value Δ_ν can be determined, if errors and noises of analogue components are known. Value Δ_ν also can be assessed from the condition that MSE P_k of conversion errors at the threshold cycle $k = n^*$ should have the value of σ_ν^2 order. Taking into account (5), (11) and the Gaussian form of distribution of the conversion errors [19] after threshold number of cycles, one can write the relationships:

$$N_{fin} = \log_2\left(\frac{2\alpha\,\sigma_0}{\Delta_\nu}\right) \quad \Rightarrow \quad \Delta_\nu = \frac{FSR}{2^{N_{fin}}}, \tag{26}$$

$$C_\infty^{\max} = \frac{2D - \Delta_{ADC}}{2\Delta_\nu} = \frac{D}{\alpha\,\sigma_0}\left(1 - \frac{\Delta_{ADC}}{2D}\right)2^{N_{fin}} = C_1^{\max}\,2^{N_{fin}}\left(1 - 2^{-N_{ADC}}\right), \tag{27}$$

where N_{fin} is final resolution of IC ADC (ENOB) achieved in n^* cycles of conversion. Substitution of (26) into (25) under fulfilled inequality $C_\infty^{\max} / C_1^{\max} >> 1$ gives the formula:

$$C_{k+1}^{\max} = \frac{C_\infty^{\max}}{1 + 2^{-kN_{ADC}}\,\dfrac{C_\infty^{\max} - C_1^{\max}}{C_1^{\max}}} = \frac{D}{\alpha\sigma_0} \times \begin{cases} 1 & \text{for} \quad k = 0 \\ \dfrac{2^{N_{fin}}(1 - 2^{-N_{ADC}})}{1 + 2^{N_{fin} - kN_{ADC}}(1 - 2^{-N_{ADC}})} & \text{for} \quad k \geq 1 \end{cases}. \tag{28}$$

The value of Δ_ν can be also evaluated experimentally by registering the moments of termination of fast growth of ENOB and registration of corresponding conversion errors. In this case, the empirical MSE can be computed:

$$\hat{P}_{n^*} = \frac{1}{M}\sum_{m=1}^{M}\left[\; V^{(m)} - \hat{V}_{n^*}^{(m)}\right]^2 \tag{29}$$

and, according to (5), it should have a value close to the variance σ_ν^2 of summary errors at the input of amplifier A input. Substituting (29) into (5) gives the evaluation: $\Delta_\nu \approx 2\alpha\,\hat{\sigma}_\nu = 2\alpha\sqrt{\hat{P}_{n^*}}$.

The results of the analysis show a crucial role of the errors and noise in the analogue block "S&H unit - Subtractor Σ - Amplifier A - feedback DAC". Under given (required) resolution N_{fin} bits of the converter ADC, their summary power should be not greater than the value determined by (26). Fulfilment of this requirement is necessary condition for IC ADC could achieve the resolution N_{fin} bits in the minimal number of cycles n^* determined by Eq. (21).

Also promising directions of the conversion algorithm improvement are the corrections of Eq. (3) and the value of saturation factor, which can be done independent upon the noise intensity Δ_ν assessment. The concept employs the fact that de-optimisation of the algorithm is caused by non-Gaussian distribution of the quantization noise ξ_k, and its influence on the ENOB reveals only through denominator of the SNR (20) as the product $\alpha^2\sigma_\xi^2$. Simulation analysis has shown [5, 11] that increment of ENOB increases and reaches a maximum, in each cycle, if the assessment (3) of quantization noise power is reduced to the values $\overline{\sigma}_\xi^2 = \gamma\sigma_\xi^2 = \gamma\Delta_{ADC}^2/12$. Optimal values $\gamma^{opt} \sim 0.4 \div 0.5$ depending on the resolution of the pre-converter ADC_{In} [5]. A similar improvement of ENOB can be achieved by heuristic selection of the saturation factor α. However, this method of IC ADC optimisation does not guarantee full utilisation of resources of the hardware and software for improvement of the conversion performance.

The discussed methods of optimisation of the IC ADC give sufficiently close numerical evaluations for sub-optimal gains $C_1^{\max},...,C_n^{\max}, L_1^{\min},...,L_n^{\min}$. For this reason, each of these methods may provide the designers with information enabling them to make proper project

decisions. If the requirements to utilisation of IC ADC elements are weakened, the gains $C_1^{\max},...,C_n^{\max}$ can be somewhat reduced. Then close to sub-optimal gains can be chosen heuristically by the assigning them values somewhat greater than degrees of two in known prototypes. The performance of so chosen version of IC ADC can be evaluated in simulations and compared with a prototype, as well as with other versions of the new converter.

Finally, we should note the perspective possibility to improve their characteristics common for every IC ADC, by modification of the computing part of algorithms taking into account the correlations between the samples of the input signal. For instance, if the sequence of samples is Markovian and Gaussian, then its mathematical model is determined by distributions [21]:

$$p(V^{(1)}) = \frac{1}{\sigma_0\sqrt{2\pi}}\exp\left[-\frac{(V^{(1)}-V_0)^2}{2\sigma_0^2}\right], \tag{30}$$

$$p(V^{(m)} \mid V^{(m-1)}) = \frac{1}{\sigma_0\sqrt{2\pi(1-\rho^2)}}\exp\left[-\frac{(V^{(m)}-\rho V^{(m-1)})^2}{2\sigma_0^2(1-\rho^2)}\right]. \tag{31}$$

In this case, the conditional distribution of each sample followed by the sample with the computed final code $\hat{V}_{fin}^{(m-1)}$ and known final MSE P_{fin} has the form:

$$\begin{aligned} p(V^{(m)} \mid \hat{V}_{fin}^{(m-1)}) &= \int_{-\infty}^{\infty} p(V^{(m)} \mid V^{(m-1)}) p(V^{(m-1)} \mid \hat{V}_{fin}^{(m-1)}) dV^{(m-1)} = \\ &= \frac{1}{\sqrt{2\pi[\sigma_0^2(1-\rho^2)+P_{fin}]}}\exp\left\{-\frac{(V^{(m)}-\rho\hat{V}^{(m-1)})^2}{2[\sigma_0^2(1-\rho^2)+P_{fin}]}\right\} \end{aligned} \tag{32}$$

Equation (32) determines optimal initial conditions for algorithm (2), (4), (17), (18). Namely, for each $m = 1, \ldots, M$, they should have the values $\hat{V}_0^{(m)} = \rho\hat{V}_{fin}^{(m-1)}$ and $P_0^{(m)} = \sigma_0^2(1-\rho^2)+P_{fin}$. Introduction of corresponding changes in re-starting the converters at the end of each sample conversion will increase the rate of conversion and range of IC ADC applications, in particular, for the conversion of non-stationary signals with the large and fast changes of magnitude.

6. DISCUSSION OF RESULTS AND CONCLUSIONS

The results of research show that transition to the long-bit word computing units enables both “intellectualisation” of CADC’s and development of efficient theoretical and simulation support for IC ADCs design and analysis. Relationships (2), (4), (17), (18) and their generalised version (2), (4), (13)-(15) from the basis for initial analysis, explanation of the effects, as well as for further optimisation and design of different classes of intelligent converters with improved characteristics. The field of applications of the approach is analytical support of system decisions at the initial stage of design. It can be used also for the prognosis of results of laboratory experiments with the hardware prototypes of the IC ADC, as well as for explanation of appearing discrepancies and their corrections.

The considered approach permits to define close-to-optimal structure, methods of

realisation and parameters of main components of the analogue and digital parts of IC ADC, which ensures close to theoretically achievable resolution and speed of conversion. Realisation of IC ADC according to these recommendations provides the close to full utilisation of resources of their analogue elements and software that diminishes the cost, sizes and energy consumption of the converters.

An important result for application is established in simulation experiments high closeness of the theoretically expected and experimental evaluations of IC ADC resolution (ENOB). The developed method of simulation analysis enables accurate and fast investigation of the effects caused by different factors influencing the quality of conversion. Moreover, simulations permit to solve the tasks unsolvable analytically, that permits to replace the theoretical research by not less accurate, fast and low-cost simulation analysis. Simulations allow fast verification of the efficiency of different corrections of initial version of IC ADC and choice of the version most answering to the goals of the project. They can be used also for the prediction and explanation of results of the experiments with the hardware prototypes of the IC ADC, as well as for the analysis and correction of unexpected effects. Results of corresponding investigations are presented in [4-12].

It is necessary to notice that one of the most urgent questions of ADC design and manufacturing remains a development of commonly accepted list of adequate characteristics of the conversion quality, as well as of also commonly accepted methods of their measurement [16]. This task is not less important and even more complex in IC ADC design, where distribution of the conversion errors differs from distribution of errors in non-iterative ADC. The results presented in the paper enable a development of adequate and convenient for applications measures of conversion quality and testing procedures.

Different possibilities of IC ADC realization - as an independent unit or as an analogue unit connected to the microprocessor or integrated into its architecture - ensure a very wide scope of IC ADC applications (as low-cost ADC arrays and matrices, among others).

The results presented in the paper both explain the sources of potential advantages of IC ADC and put the basis for their practical realisation. The considered approach can be used for the development of other classes of iterative intelligent ADCs. Analytical results of the work can be applied also to design of highly-efficient “intelligent” adaptive signal processing and measurement systems.

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