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APPLICATION OF DIGITAL DITHER TO REDUCTION OF FEEDBACK D/A CONVERTERS INFLUENCE ON INTELLIGENT CYCLIC A/D CONVERTERS PERFORMANCE*

The effect of termination of resolution growth, common for cyclic analogue-to-digital converters (CADCs) the, which appears after a definite (threshold) number of the conversion cycles, is investigated in the paper. The effect is caused by the finite resolution of the D/A converter (DAC) in the feedback chain. In an “intelligent” CADC (IC ADC, [1-6]), the growth of resolution can be restored by adding the digital dithering signal to the signal at the input of the feedback DAC. The dependence of the rate of restored growth of resolution on the distribution and amplitude of the dithering signal is investigated. The results of analysis are verified in advanced simulation experiments.

Keywords: cyclic A/D converters, resolution, ENOB, digital dither

1. INTRODUCTION

The results of investigations presented in works [1-6] and others show the possibility to design and realize a new class of “intelligent” cyclic A/D converters (IC ADCs). The particular feature of IC ADCs distinguishing them from the conventional CADCs [7, 8] is the replacement of the digital binary logic elements in their code forming (digital) parts by simple computing units permitting to compute the codes in the form of long binary words of the fixed length N_{comp} (e.g. $N_{comp} = 16, 24$ or 32 -bits). The computing of codes as well as the optimal adaptive adjusting of the analogue part of IC ADC are realised using sub-optimal adaptive algorithms based on the approach presented in [9,10]. These algorithms take into account the distribution and parameters of the internal and external noise, input signals, as well as of components of the analogue part of IC ADC. Adjusting of the analogue part of the IC ADC is carried out in a way eliminating, at each cycle of conversion, its possible overloading with the guaranteed confidence level (probability) $1 - \mu$ ($\mu = 1$). Unlike the conventional CADCs, IC ADCs utilize more efficiently the resources of the analogue and digital parts.

In this paper, the empirically revealed effect of termination of IC ADC resolution growth after a definite “threshold” number of cycles of the sample conversion is investigated. A similar effect called also “resolution saturation” exists in each known cyclic converter (see also [11]). The results of preliminary analysis [12] showed that the effect is caused by the finite resolution of the internal feedback D/A converter (DAC_{ln} , see Fig. 1) always present in CADC architecture. Additional investigations [12] permitted us to conclude that introduction of a small digital additive noise (dither) at the feedback D/A converter input restores a monotonic growth of resolution at a greater number of cycles than the threshold number.

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Below, the results of a deep analysis of the reasons of IC ADC resolution saturation and of the application of digital dither as a method of restoring its growth are presented. Also the influence of distributions and parameters of dither signals on the rate of IC ADC resolution growth for a number of conversion cycles greater than the threshold number is investigated. The paper develops and generalizes the results of the investigation presented in [12].

2. PRINCIPLES OF IC ADC OPERATION

The background of IC ADC operation can be easily explained on the basis of the general diagram of an IC ADC presented in Fig.1, which illustrates the principles of its conversion (see also e.g. [1-4]).

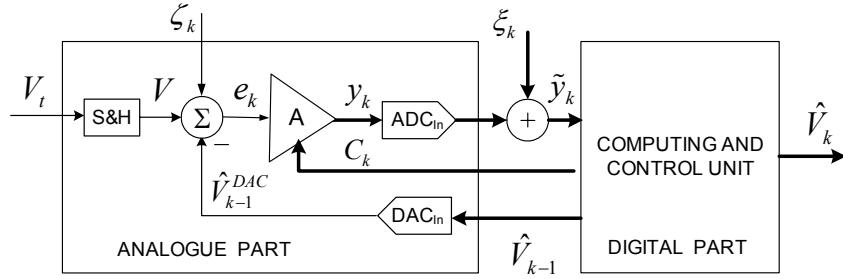


Fig.1. General architecture of the intelligent cyclic A/D converter.

The input voltage signal V_t is transformed in the sample-and-hold (S&H) block into a rectangular pulse sequence $V^{(m)} = V(mT)$, $m = 1, 2, \dots$, (T is the sampling interval). Further conversion of each sample $V^{(m)}$ is performed in $n = T/\Delta t_0$ cycles, independently of the results of the previous sample conversion (Δt_0 is the duration of a single conversion cycle). During each sample interval T , the S&H block maintains a constant voltage $V^{(m)}$ at the input of the subtractor (Σ).

In each k -th cycle ($k = 1, 2, \dots, n$) of the sample $V^{(m)} = V$ conversion (index m is further omitted), the subtractor Σ forms the residual signal $e_k = V - \hat{V}_{k-1}^{DAC} + v_k$, which is routed to the input of the amplifier (A) with the controlled gain C_k . Variable v_k denotes the sum of the analogue noise of the feedback D/A converter (DAC_{in}), the S&H block, the subtractor Σ , and possible external noise. The amplified analogue signal $C_k e_k$ is routed to the input of the internal coarse A/D converter ADC_{in}. The binary N_{ADC} -bit code \tilde{y}_k ($N_{ADC} = 1 \div 6$ bits) formed by ADC_{in} is processed in the computing and control unit (CCU) which computes the intermediate \hat{V}_k and the final \hat{V}_n estimates (codes) of the input sample in the form of N_{comp} -bit binary words ($N_{comp} = 16, 24$ or 32 -bits depending on the required final resolution of the converters). The computing is carried out according to the following relationship:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k \quad (k = 1, 2, \dots, n). \quad (1)$$

Observations \tilde{y}_k in (1) are formed according to the non-linear model:

$$\tilde{y}_k = \begin{cases} C_k e_k + \xi_k & \text{for } |e_k| \leq D/C_k \\ D \operatorname{sgn}(e_k) + \xi_k & \text{for } |e_k| > D/C_k \end{cases}, \quad (2)$$

which approximates the step-wise transfer function of the IC ADC's analogue part (see Fig. 2a). Coefficient C_k in (2) is the gain of amplifier A and L_k in (1) is the digital N_{comp} -bit gain numerically connected with C_k . Noise ξ_k in (2) is the quantization noise whose variance is evaluated according to the commonly used formula [7, 13]: $\sigma_\xi^2 = \Delta^2 / 12 = D^2 \cdot 2^{-2N_{ADC}} / 3$, where $D = \text{FSR}/2$ is half of the full scale range (FSR) of ADC_{In} , Δ is its quantization interval, and N_{ADC} its resolution.

The digital CCU in IC ADC computes the N_{comp} codes \hat{V}_k by adding the N_{comp} -bit binary word $L_k \tilde{y}_k$ to the previous estimate \hat{V}_{k-1} and replaces the previous N_{comp} -bit estimate \hat{V}_{k-1} , stored in the CCU memory, by the new estimate of the same length. This new estimate \hat{V}_k is routed to the input of the N_{DAC} -bit feedback DAC_{In} and its analogue equivalent $\hat{V}_k^{DAC} = \hat{V}_k + v_k^{DAC}$ formed by DAC_{In} is routed to the second input of the subtractor Σ , and the next $k+1$ -th cycle of conversion begins. Close-to-optimal (sub-optimal) values of the analogue gains C_k of amplifier A and digital gains L_k which minimise the mean square error (MSE) of conversion can be determined, for each $k = 1, 2, \dots, n$, by solution of the corresponding optimization task [9, 10]. The minimization is performed under the condition that the probability of IC ADC saturation is not greater than a given small value μ . For an IC ADC, sub-optimal values of the gains C_k and L_k are determined by the formulas, [1-6, 10]:

$$L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_v^2} = \left(1 - \frac{P_k}{P_{k-1}}\right) \frac{1}{C_k}, \quad C_k = \frac{D}{\alpha \sqrt{\sigma_v^2 + P_{k-1}}} \quad (3)$$

and the MSE of conversion P_k is calculated according to the formulas:

$$\frac{1}{P_k} = \frac{1}{P_{k-1}} + \frac{1}{\sigma_\xi^2 + C_k^2 \sigma_v^2} \quad \text{or} \quad P_k = \frac{\sigma_\xi^2 + C_k^2 \sigma_v^2}{\sigma_\xi^2 + C_k^2 (\sigma_v^2 + P_{k-1})} P_{k-1}. \quad (4)$$

Initial conditions for algorithm (1)-(4) $\hat{V}_0 = V_0$ and $P_0 = \sigma_0^2$, where \hat{V}_0 , σ_0^2 are the mean value and maximal permissible power of the input signal, respectively. Parameter α in (3) is determined by the accepted probability μ of IC ADC overloading, and satisfies the equation: $\Phi(\alpha) = (1 - \mu)/2$, where $\Phi(\alpha)$ is the Gaussian error function. For an IC ADC constructed according to the algorithm (1)-(4), the performance of the converter attains values close to the theoretically achievable boundary established by (4) (see also [1-6]).

The resolution of the sub-optimal IC ADC built according to (1)-(4), more accurately called the effective number of bits (ENOB) [13,14], is given by the relationship [6]:

$$N_k = \frac{1}{2} \log_2 \left(\frac{\sigma_0^2}{P_k} \right) = N_{k-1} + \frac{1}{2} \log_2 (1 + Q^2) - \frac{1}{2} \log_2 \left(1 + Q^2 \frac{\sigma_v^2}{\sigma_v^2 + P_{k-1}} \right), \quad (5)$$

where $Q^2 = C_k^2 E(e_k^2) / \sigma_\xi^2 = (D / \alpha \sigma_\xi)^2 = 3 \cdot 2^{2N_{ADC}} / \alpha^2$ is the signal-to-noise ratio (SNR) at the ADC_{In} output. In the cyclic converters, the noise v_k is usually small, that is $\sigma_v^2 = \sigma_0^2$. In this case, there always exists the initial interval $1 \leq k < n^*$, where MSE of conversion decreases and ENOB increases with maximal rate [6]:

$$P_k = P_{k-1}(1+Q^2)^{-1} = \sigma_0^2(1+Q^2)^{-k}, \quad (6)$$

$$N_k = \frac{k}{2} \log_2(1+Q^2), \quad (7)$$

respectively. According to (4) and (5), ENOB of the sub-optimal IC ADC grows, for $k > n^*$, monotonically as a logarithmic function of k and independently from the values of converter parameters (overloading excluded), because a difference of logarithms in (5) is always positive. The threshold point n^* of transition from the linear to logarithmic rate of ENOB growth can be evaluated by the formula [10]:

$$n^* = \frac{1}{\log(1+Q^2)} \log\left(\frac{\sigma_0^2}{\sigma_v^2}\right). \quad (8)$$

3. TERMINATION OF ENOB GROWTH

The computer analysis of an IC ADC with feedback DAC_{ln} modelled by the stepwise transfer function (Fig 2) has shown that the growth of ENOB is terminated after a threshold number of cycles n^* . Apart from the analysis of the effect, simulation experiments permitted to develop methods of its elimination. Both ADC_{ln} and DAC_{ln} were modelled by stepwise (ideal) transfer functions (see Fig. 2a, b). The analogue part of IC ADC was modelled according to the diagram of IC ADC presented in Fig. 1, taking into account the finite input range $[-D, D]$ of the internal converter ADC_{ln} .

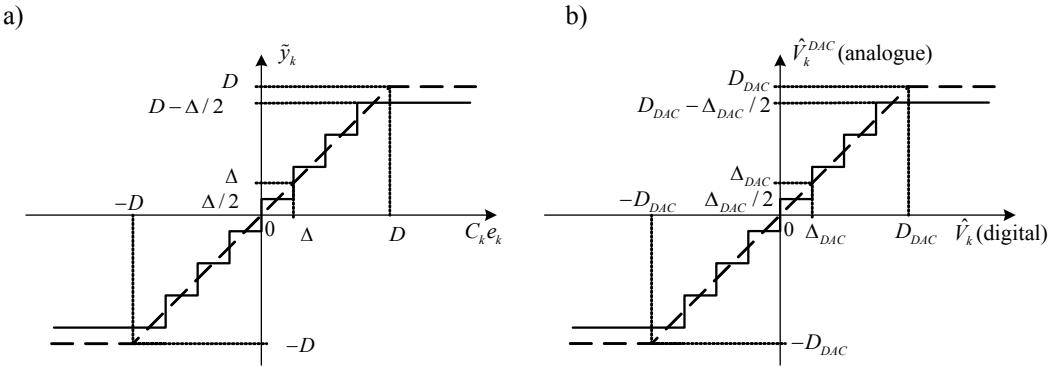


Fig.2. Transfer functions used for modelling: a) of the internal ADC_{ln} , b) of the feedback DAC_{ln} .

Two types of testing input signals were used: sequences of random Gaussian mutually independent samples $V^{(m)}$ ($m = 1, \dots, M$) and digital realizations of a sine wave $V^{(m)} = A \sin(2\pi f_0 m)$, where f_0 is the normalized frequency of the signal, and $A = D_{DAC} - \Delta_{DAC}$ - its amplitude. IC ADC resolution (ENOB) \hat{N}_k was measured using empirical evaluation of MSE of conversion according to the formulas:

$$\hat{N}_k = \frac{1}{2} \log_2 \frac{\sigma_0^2}{\hat{P}_k}, \quad \hat{P}_k = \frac{1}{M} \sum_{m=1}^M (\hat{V}_k^{(m)} - V_k^{(m)})^2, \quad (9)$$

where $\hat{V}_k^{(m)}$ are the estimates of the m -th sample at the k -th cycle of conversion. Simulation experiments were carried out for the following parameters: $D_{DAC} = 5$, $\alpha = 4$, $D = 1.25$, $V_0 = 0$, $\sigma_0 = 1.25$, $N_{ADC} = 2$ or 4 bits, $N_{DAC} = 8, 12, 16$ bits, $M = 5000$ samples.

It was assumed that the dominating component of analogue noise v_k at the amplifier input is the noise of the feedback DAC_{In} conditioned by its finite resolution N_{DAC} . Then, the variance σ_v^2 in (3), (4) can be evaluated as follows:

$$\sigma_v^2 = \Delta_{DAC}^2 / 12 = D_{DAC}^2 \cdot 2^{-2N_{DAC}} / 3, \quad (10)$$

where the output range of the DAC_{In} is equal to the input range of IC ADC, the value $\Delta_{DAC} = 2D_{DAC} / 2^{N_{DAC}}$ is the DAC_{In} quantisation interval and is the resolution of DAC_{In}.

In the first series of experiments, changes of trajectories $\hat{N}_k = \hat{N}(k)$ of the empirical ENOB (9) depending on different values N_{ADC} and N_{DAC} were investigated. The plots presented in Fig. 3 show these trajectories under different DAC_{In} resolutions $N_{DAC} = 8, 12, 16$ bits (corresponding plots in the figures - from the bottom to the top). Plots in Fig. 3a refer to an IC ADC employing internal ADC_{In} with resolution $N_{ADC} = 2$ bits, and in Fig. 3b – with resolution $N_{ADC} = 4$ bits. Continuous lines correspond to the ENOB trajectories obtained under the assumption that DAC_{In} is the main source of errors and dominates other components of the analogue noise v_k . Dashed lines refer to the experiments carried out assuming that DAC_{In} has high resolution and the dominating component of the noise v_k is Gaussian white noise. The power of this noise was taken equal to the power of DAC_{In} errors (10). The obtained plots (dashed lines) coincide with the theoretical evaluation calculated according to (5).

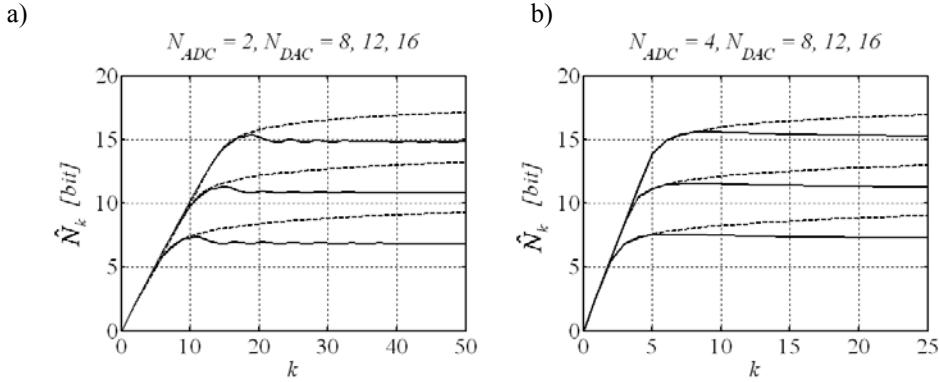


Fig.3. ENOB of IC ADC as a function of number of cycles for different DAC_{In} resolution and (a) $N_{ADC} = 2$, (b) $N_{ADC} = 4$, for stepwise (continuous lines) and Gaussian (dashed lines) models of DAC_{In}.

The results of experiments show that termination of ENOB growth is caused by the finite resolution of DAC_{In} which becomes the main source of errors when the power of D/A conversion errors is much greater than the power of other components of the noise v_k . It was also established that application of very low-bit ADC_{In} ($N_{ADC} \leq 3$) causes the appearance, after a threshold number of cycles, of small disappearing oscillations around the limit value of ENOB (Fig. 3a). This effect can be useful in practical applications and requires additional consideration.

Figure 4 presents the FFT spectra of the converted sine wave obtained using the stepwise and Gaussian models of the feedback noise. The input sine wave parameters: $A = 4.9976$, $M = 1024$, $f_0 = 53/1024$. One can easily see that in the case of the stepwise model of DAC_{In},

both additional harmonics appear and the noise floor increases in the spectra of converted signals in comparison with the case of feedback Gaussian noise of the same power.

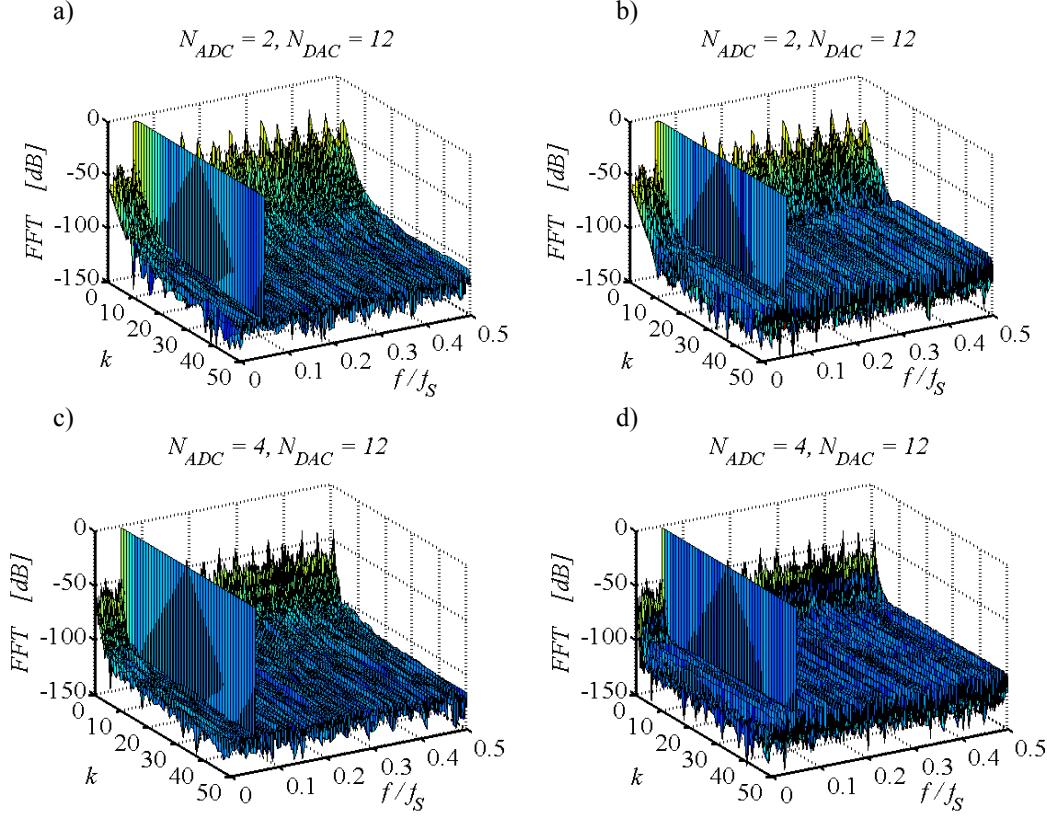


Fig.4. FFT spectra of the converted sine wave as a function of cycles number for $N_{DAC} = 12$ and (a-b) $N_{ADC} = 2$, (c-d) $N_{ADC} = 4$ for Gaussian (a, c) and stepwise (b, d) models of DAC_{in} quantization errors.

Investigation of the reasons of termination of ENOB growth was carried out in an independent series of simulation experiments with IC ADC where DAC_{in} was modelled using the ideal step-wise transition function presented in Fig. 2b. To clarify the analysis, other components of the noise v_k were excluded from consideration. Plots in Fig. 5 present trajectories of empirical estimates $\hat{V}_k = \hat{V}(k)$, (continuous lines) and trajectories $\hat{V}_k^{DAC} = \hat{V}^{DAC}(k)$ of the signal at the DAC_{in} output (dashed lines).

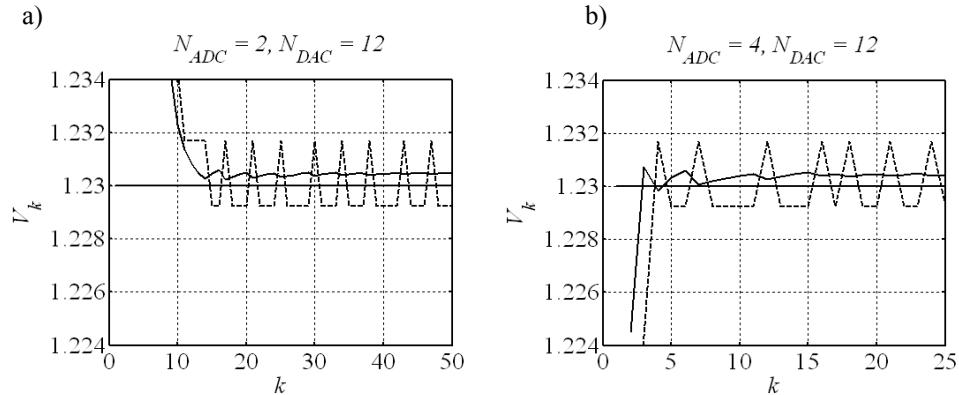


Fig.5. Typical runs of estimates \hat{V}_k (continuous lines) and analogue signals \hat{V}_k^{DAC} at the DAC_{in} output (dashed lines) for $N_{DAC} = 12$ and (a) $N_{ADC} = 2$, (b) $N_{ADC} = 4$.

The obtained results show that the estimates \hat{V}_k do not converge to the real value V of the input sample ($V = 1.23$, bold horizontal lines in Fig. 4), but to the middle point $V_{\Delta/2} \approx 1.2305$ of the DAC_{in} quantization interval containing the value V of the input sample. The reason of the effect is the fact that, for the greater number of cycles $k \geq n^*$, the analogue signal \hat{V}_{k-1}^{DAC} at the DAC_{in} output takes only two values, equal to the upper and lower boundaries of the quantization interval referring to the value V ($\hat{V}_{k-1}^{DAC} = 1.2292$ or 1.2317 , respectively). This results in the appearance of constant bias of the estimates \hat{V}_k , which causes the termination of growth of IC ADC resolution. Beginning with $k = n^*$ ($n^* \approx 11$ for $N_{ADC} = 2$, $N_{DAC} = 12$ and $n^* \approx 4$ for $N_{ADC} = 4$, $N_{DAC} = 12$, which coincides with the numerical evaluation according to (8)), the MSE of estimates \hat{V}_k reaches values comparable with quantization errors of DAC_{in} . Assuming that values $\hat{V}_k^{(m)} - V^{(m)}$ referring to different input samples are distributed uniformly in the range $\pm \Delta_{DAC}/2$, one can evaluate the achievable resolution - the upper value of ENOB:

$$N_{k|k>n^*} = \frac{1}{2} \log_2 \left(\frac{\sigma_0^2}{\sigma_v^2} \right) = N_{DAC} - \frac{1}{2} \log_2 \left(\frac{\alpha^2}{3} \right). \quad (11)$$

This relationship gives a permit to evaluate the achievable ENOB of the IC ADC in the simplest way. So, for $\alpha = 4$, Eq. (11) gives the assessment: $N^{limit} = N_{DAC} - 1.21 \approx 10.8$ which is close to the empirical limit values of ENOB in Fig. 3.

Resumé: Termination of IC ADC resolution growth is conditioned by oscillations of the analogue signal \hat{V}_{k-1}^{DAC} at the DAC_{in} output appearing after the threshold number of conversion cycles ($k > n^*$). The necessary condition of their appearance is the finite resolution of DAC_{in} and the small, in comparison with the D/A conversion errors, power of the analogue noises at the amplifier A input.

4. INFLUENCE OF DITHER SIGNAL CHARACTERISTICS ON RESTORATION OF IC ADC RESOLUTION GROWTH

The results of work [12] show that the terminated growth of ENOB in IC ADC can be restored, if undesired oscillations of the values of the analogue signal \hat{V}_{k-1}^{DAC} at the DAC_{in} output will be removed. This can be done by adding, for $k > n^*$, a digital dither signal d_k to the signal at the DAC_{in} input. This destroys the regular oscillations of the analogue signal \hat{V}_{k-1}^{DAC} at the DAC_{in} output and in consequence removes the bias of estimates \hat{V}_k and restores the growth of ENOB. Further investigations show that the rate of restored growth of ENOB depends on the form or distribution of the dither signal and its amplitude. The influence of these factors was analysed in an independent series of simulation experiments carried out for the most frequently used [15] classes of dither signals, namely (see also Figs. 6a-d):

- Gaussian dither - generated digitally as sequences of Gaussian random values with the standard deviation $\sigma_\eta = \eta \Delta_{DAC}$,
- uniform dither - generated as sequences of random values uniformly distributed in the interval $[-\eta \Delta_{DAC}, \eta \Delta_{DAC}]$,
- random bipolar dither - generated as sequences of randomly equiprobable constant values $-\eta \Delta_{DAC}$ or $\eta \Delta_{DAC}$,

- deterministic bipolar dither - generated as sequences of constant values $-\eta\Delta_{DAC}$ or $\eta\Delta_{DAC}$ changing the sign in each cycle of conversion.

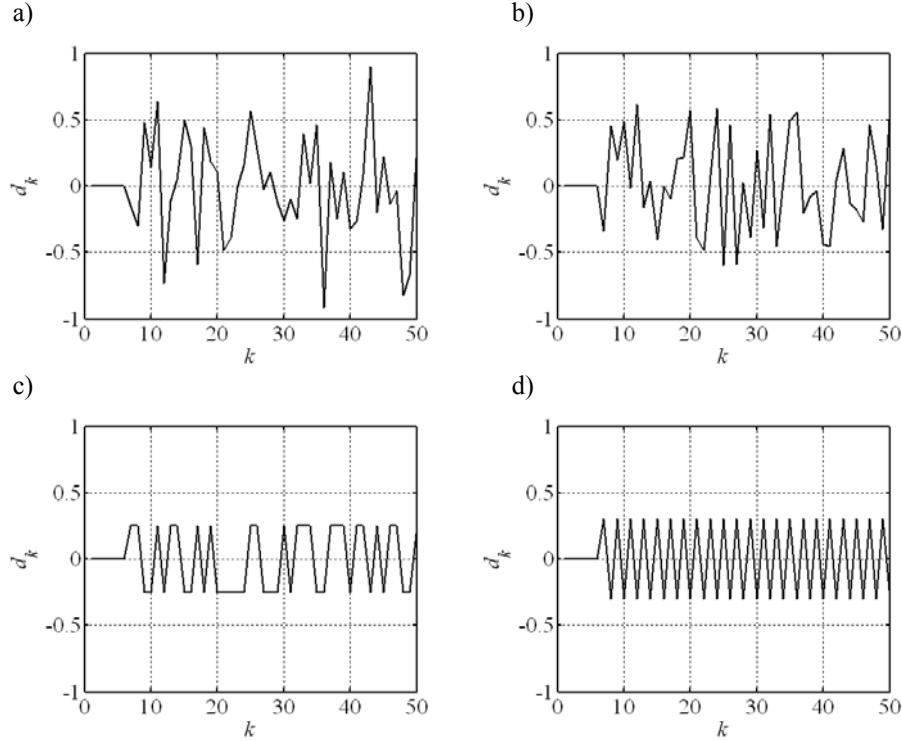


Fig.6. Typical realizations of the considered dither signals (normalized in Δ_{DAC}): (a) Gaussian dither, (b) uniform dither, (c) random bipolar dither, (d) deterministic bipolar dither.

In all cases listed above, the coefficient η determines the intensity (amplitude) of the dither signal. The influence of the form, distribution and the intensity of the dither on IC ADC's performance was analyzed using, as its efficiency measure, the increment of ENOB:

$$\Delta\hat{N}_k = \hat{N}_k^{dith} - \hat{N}_k = \log\left(\frac{\hat{P}_k}{\hat{P}_k^{dith}}\right), \quad (12)$$

between the ENOB \hat{N}_k^{dith} of an IC ADC with dither and ENOB \hat{N}_k of an IC ADC without dither. MSE \hat{P}_k^{dith} and ENOB \hat{N}_k^{dith} in (12) are computed according to Eq. (9). The general concept and parameters of experiments were the same as in Section 3.

In the first series of experiments, the dependence of ENOB on the parameters of the Gaussian dither was investigated. In Figure 7, plots of the increment of ENOB $\Delta\hat{N}_k = \Delta\hat{N}(k, \eta)$ obtained in the simulation are presented.

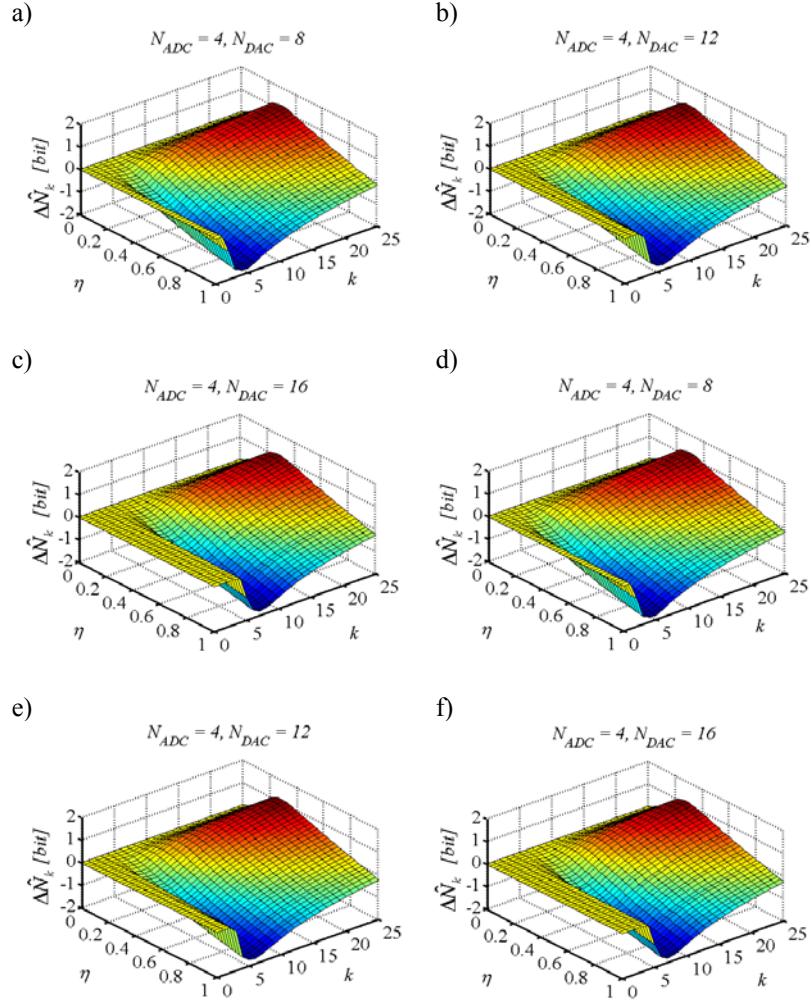


Fig. 7. Dependencies of increment of ENOB intensity coefficient η and number of cycles for the Gaussian dither: (a-c), (d-f).

As follows from Fig. 7, the increment of ENOB depends on the values of the intensity coefficient η and the most efficient values η^* which maximize the increment, are $\eta^* = 0.4$ for $N_{ADC} = 2$, and $\eta^* = 0.3$ for $N_{ADC} = 4$, respectively. Simultaneously, introduction of the dither causes a small, quickly disappearing diminution of ENOB after a threshold number of cycles $k > n^*$ (see also Fig. 9). This temporary effect is a consequence of introduction of additional noise, and is more intensive for greater values of η .

Figure 8 presents, similarly to Fig. 5, trajectories of the digital estimate \hat{V}_k changes for a growing number of conversion cycles (continuous lines). Corresponding trajectories of the signal \hat{V}_{k-1}^{DAC} at the DAC_{In} output are shown as dashed lines. The values of dither intensity coefficient η were taken as equal to the most efficient values η^* determined in previous experiment. The results of experiments show that the application of dither destroys the symmetry of \hat{V}_{k-1}^{DAC} oscillations, as well as causes a (rare) appearance of the next, nearest to the input sample value V , values of the signal \hat{V}_{k-1}^{DAC} at the DAC_{In} output. This restores the convergence of estimates \hat{V}_k to the actual value of the sample $V = 1.23$ (bold horizontal line), instead to the centre of the quantization interval of DAC_{In} (compare Fig. 5).

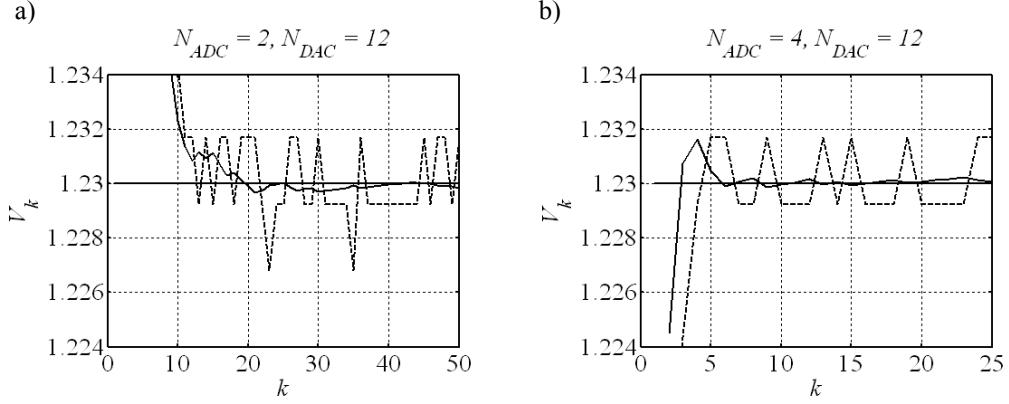


Fig.8. Typical runs of estimates \hat{V}_k (continuous lines) and analogue values \hat{V}_{k-1}^{DAC} at the DAC_{in} output (dashed lines) for IC ADC with Gaussian digital dither for $N_{DAC} = 12$ and (a) $N_{ADC} = 2$, (b) $N_{ADC} = 4$.

The improvement of ENOB of the IC ADC due to the application of Gaussian digital dither is shown in Fig. 9. The dotted lines refer to an IC ADC with dither ($\eta = \eta^*$), and the continuous lines - to the same IC ADC without dither ($\eta = 0$). For $k \geq n^*$, the limit values of ENOB can be evaluated by the approximate relationship similar to (11):

$$N_{k|k>n^*} = N_{DAC} - \frac{1}{2} \log_2 \left(\frac{\alpha^2}{3} \right) + \frac{1}{2} \log_2 \left(\frac{k}{n^*} \right), \quad (13)$$

which gives the numerical assessments of ENOB close to the measured ones.

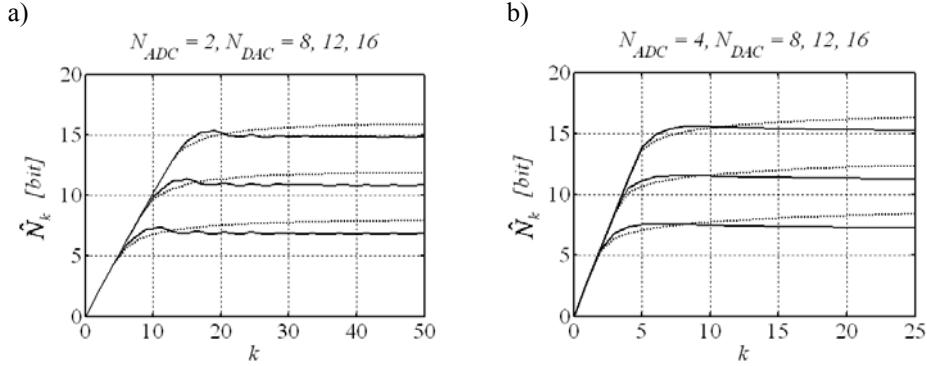


Fig.9. ENOB of IC ADC without usage of dither (continuous lines) and IC ADC applying Gaussian digital dither (dotted lines): (a) $N_{ADC} = 2$ and $\eta^* = 0.4$, (b) $N_{ADC} = 4$ and $\eta^* = 0.3$.

Figure 10 present the FFT spectra of a converted sine-wave signal computed for IC ADC with the Gaussian dither. As in Section 3, IC ADCs with different ADC_{in} resolution $N_{ADC} = 2$ $N_{ADC} = 4$ were analysed. Dithering signals were generated with the most efficient values of intensity: $\eta^* = 0.4$, $\eta^* = 0.3$, respectively. Comparison with the plots presented in Figs. 4b, d shows that the introduction of digital dither diminishes the amplitude of undesired harmonic components and decreases the noise floor in the spectra of signals at the IC ADC output.

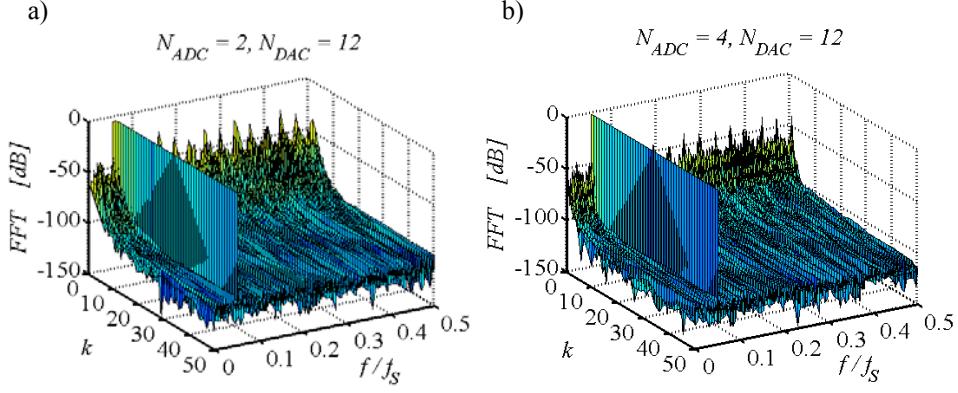


Fig.10. FFT spectra of converted sine wave as a function of cycles number for IC ADC with Gaussian digital dither, $N_{DAC} = 12$ and (a) $N_{ADC} = 2$ and $\eta^* = 0.4$, (b) $N_{ADC} = 4$ and $\eta^* = 0.3$.

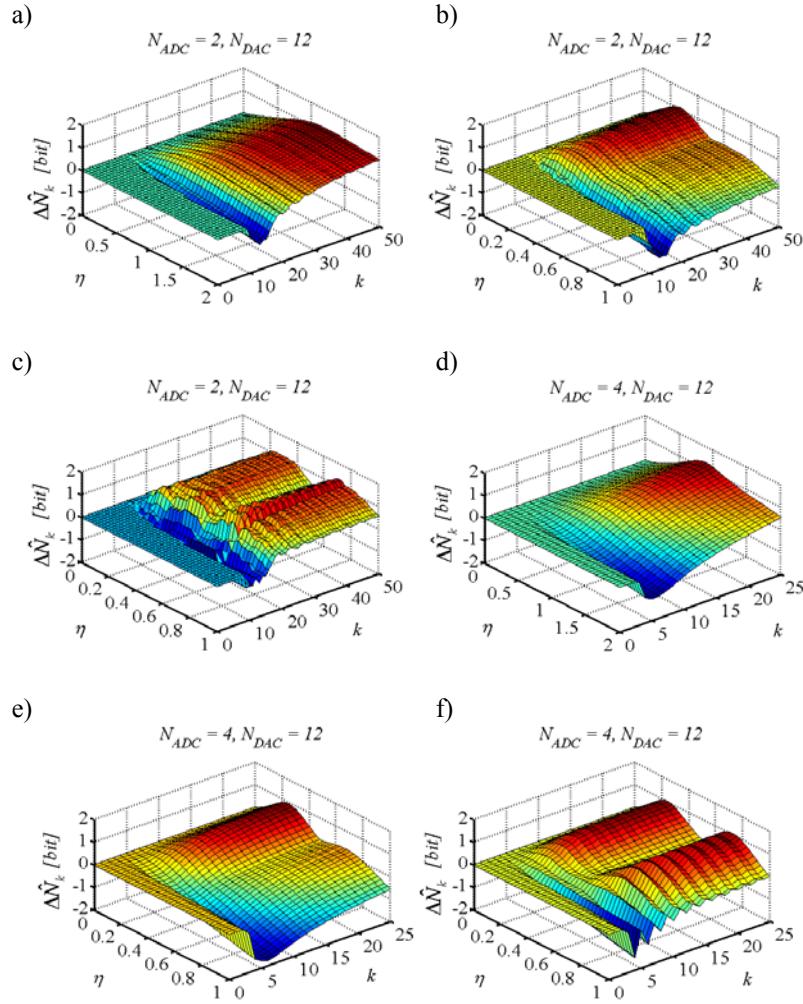


Fig.11. Differences $\Delta\hat{N}_k = \hat{N}_k^{dith} - \hat{N}_k$ between ENOB of IC ADC with digital dither and without dither obtained for different dither classes: (a, d) - random uniform, (b, e) - random bipolar, (c, f) - deterministic bipolar.

Analysis of effects caused by application of other classes of digital dither listed above was carried out in the same way as for Gaussian dither. Fig. 11 shows the results of experiments carried out for the models of IC ADC with different resolutions of ADC_{In} : plots in the upper row correspond to the ADC_{In} with resolution $N_{ADC} = 2$ bits and in the lower row are obtained

under $N_{ADC} = 2$ bits. Plots in Figs. 11a and 11d show changes of the current values of increment $\Delta\hat{N}_k = \hat{N}(k, \eta)$ in the case of application of the uniformly distributed dither (see Fig. 6b), in Figs. 11b and 11e - obtained using random bipolar dither (see Fig. 6c), and in Figs. 11c and 11f - obtained using deterministic bipolar dither (see Fig. 6d).

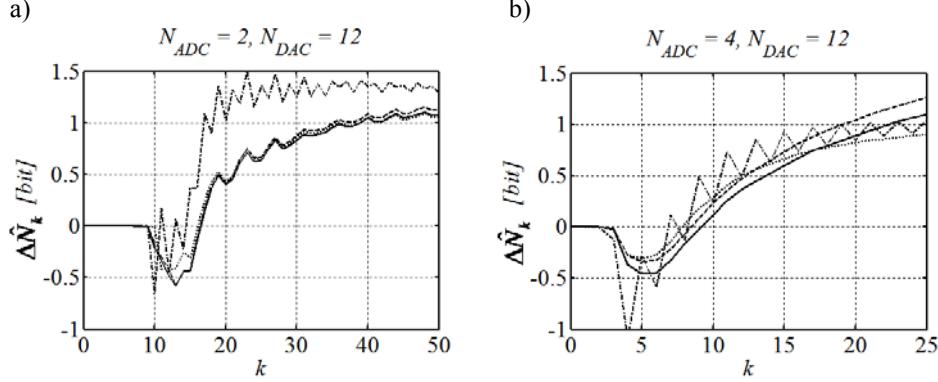


Fig.12. Changes of increment $\Delta\hat{N}_k = \hat{N}_k^{dith} - \hat{N}_k$ for different dither forms: Gaussian (continuous lines), uniform (dashed lines), random bipolar (dotted lines) and deterministic bipolar (dash-dotted lines) for the most efficient values of dither intensity coefficients $\eta = \eta^*$ and for: (a) $N_{ADC} = 2$, (b) $N_{ADC} = 4$.

The results show that for $k > n^*$, the maximal rate of the ENOB increment can be reached for the values of the dither intensity coefficients presented in Table1:

Table 1.

Resolution	Uniform dither	Random bipolar dither	Deterministic bipolar dither
$N_{ADC} = 2$ bit	$\eta^* = 1.25$	$\eta^* = 0.25$	$\eta^* = 0.7$
$N_{ADC} = 4$ bit	$\eta^* = 0.9$	$\eta^* = 0.25$	$\eta^* = 0.75$

Figure 12 presents typical runs of the maximally fast growth of ENOB increment obtained with $\Delta\hat{N}_k = \Delta\hat{N}(k)$ the most efficient values $\eta = \eta^*$ for different dither forms. Continuous lines in Fig.12 refer to an IC ADC with Gaussian dither, and dashed, dotted and dash-dotted lines to an IC ADC with uniform, random bipolar and deterministic bipolar digital dithers, respectively. A comparison of the plots permits to conclude that the improvement of the resolution of IC ADC weakly depends on the distribution of the random dither signal. However, as it follows from Figs. 12a for an IC ADC using the low-bit ADC_{In} ($N_{ADC} = 2$), the application of deterministic bipolar dither (see Fig. 6d) gives significantly better results than the application of the random dither signals. The local small decrease of ENOB, common for all discussed plots after the n^* -th cycle of conversion is caused by the local increase of ENOB noted in Sect. 3 for $k > n^*$ (see Fig. 3), and by the deterioration of estimation accuracy appearing in these cycles as a reaction to the dithering signal.

It is worth to notice that the application of the analogue dither in the case of an IC ADC does not improve its resolution. Being applied at the input of the converter, an analogue dither signal acts as weak additive noise. If the dither signal is added to the signal at the input of amplifier A, it acts as a component of the analogue noise v_k and may only decrease the ENOB.

5. CONCLUSIONS

The results of investigation show that the termination of resolution (ENO_B) growth after the threshold number of cycles ($k > n^*$), common for the cyclic ADCs, is caused by the bias of estimates appearing due to the finite resolution of the feedback DAC_{In}. The presented results show that in an IC ADC, this effect can be eliminated by adding a small digital dither signal to the estimates \hat{V}_{k-1} routed to the input of the feedback DAC_{In}. This restores a monotonic increase of ENOB at the post-threshold interval of conversion and permits to increase the resolution of the IC ADC by proper choice of the number of conversion cycles. The resolution of IC ADCs with digital dither can be increased until reaching values significantly greater than in conventional cyclic ADCs with the same ADC_{In} and DAC_{In} without any changes in the analogue part of the converter.

One should notice (see also [6,10]) that each additional bit in the post-threshold ($k > n^*$) interval can be achieved after a significantly greater number of cycles than in the pre-threshold interval $1 \leq k \leq n^*$, which narrows the frequency bandwidth of the converter. Nevertheless, in many practical cases this limitation is not crucial, especially in low-frequency applications.

It is established also that an efficient class of digital dither, convenient for implementation, is the deterministic sequence of bipolar constant values with the amplitude $\eta^* \Delta_{DAC}$. The most efficient value of the coefficient η^* depends on the resolution of the internal ADC_{In} and can be assessed additionally.

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