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DIGITAL-TO-ANALOG CONVERSION USING DELTA-SIGMA MODULATORS IMPLEMENTED IN VIRTEX-4 FPGA DEVICES

This paper presents some selected architectures of delta-sigma modulators which are suitable for implementation of digital-to-analog converters (DACs) in modern FPGA devices. Simulation and implementation of simple architectures of first and second order of digital-to-analog converters in FPGA chip is described. Experimental tests have been performed using the evaluation board ML401 from *Xilinx*, based on the XC4VLX25 Virtex-4 chip. The quality of DACs has been measured and described by relevant power spectrum diagrams and differential linearity functions. Detailed comparison of DAC architectures is also given in terms of used resources and maximum operating frequency. It has been shown that carefully designed delta-sigma modulators implemented using modern FPGA technology are competitive to conventional integrated DACs. Consequently, multichannel DACs and ADCs of good quality can be designed within the FPGA chip. In this way, the idea of single-chip measurement system containing all essential parts as DACs, ADCs, CPU and digital I/O becomes an interesting alternative to the classical approach based on the multi-chip and/or ASIC technology.

Keywords: delta-sigma modulation, FPGA, digital-to-analog converter

1. INTRODUCTION

Recent improvements of FPGA technology, especially its increased logical capacity, growing speed and more flexible logical structures are important factors creating a new technological platform competitive to widely used ASICs. It is of special importance in the field of digital signal processing and measurement systems, where dedicated instruments are often assembled in very small volumes. Nowadays engineers can choose between a number of modern FPGA devices like Virtex-4, Virtex-5 and Spartan-3 from *Xilinx*, Stratix II and Cyclone II from *Altera* or ProASIC3 from *Actel*. The logical capacity of these devices counted in millions of gates and operating frequencies approaching 500 MHz are good enough for implementation of complete digital systems within a single chip called SoC (*system-on-chip*). Implementation inside these structures of effective 1-bit ADCs and DACs based on the delta-sigma modulators is

also possible and relatively easy, obviously under the condition that they are designed entirely in digital form [1].

The technology of programmable devices is still improving and becomes more and more cheap, therefore new solutions and structures of DACs implemented in FPGA devices are possible. A trend towards faster and more complicated applications combined with the demand of lower cost and small power consumption causes replacement of traditional analog circuits by their digital equivalents [2]. Moreover, as mentioned above, digital circuits may be integrated within a single chip, creating a new quality – SoC. Thus, the integration of DACs and ADCs in programmable digital devices is of great importance because it is resulting in more consolidation, flexibility and cost reduction of SoCs.

The idea of digital-to-analog conversion based on delta-sigma modulation is relatively old and has been described in many papers. However, implementation of such a DAC in FPGA devices is still a challenging problem when both high accuracy and fast operation are required. In [1] the authors have presented an universal module of DAC for audio application. They simulated DAC using SIMULINK and *delsig* toolbox [3], and then they implemented DAC of third- and fifth-order in XC2V100-4 Virtex II FPGA device from *Xilinx*. The parameters of the DAC described in [1] are good, but the weak points of these solutions are: large amount of used resources and relatively low speed (maximum 51 MHz). Another paper [4] is focused on reduction of FPGA resources used by the modulator designed as a DPA (digital phase accumulator). The authors succeeded in the realization of a 16-bit modulator that occupied three macrocells of a Virtex II FPGA chip. In this solution the input signal must have a serial form, and the maximum sampling frequency must be equal to 87.5 MHz, 42.4 MHz, 20.6 MHz or 8.4 MHz depending on the 4-, 8-, 16-, or 32-bit resolution of the input signal, respectively. The cost of this architecture, which is of special importance in multichannel DACs, is low. Some simple architectures of DACs implemented in Virtex II FPGA are also shown in [5], where the author discusses practical aspects of their application. In [6] the same author presents an ADC based on the architectures described in [5].

As one can see from the brief review of references cited above, our knowledge on DAC and ADC implementation in modern FPGA chips is far from a complete, ready-to-use methodology. The authors have shown some particular architectures of DACs designed for implementation in a FPGA device (in most cases from older families), but did not compare different architectures and did not discuss their limits, especially with respect to modern FPGA technology. Hence, the last two issues are the main subjects of this paper.

2. SELECTED ARCHITECTURES OF DELTA-SIGMA MODULATORS USED IN DIGITAL-TO-ANALOG CONVERTERS

To achieve fast and high resolution analog-to-digital and digital-to-analog conversion, high order modulators and/or multibit modulators are required. Multibit modulators can be combined with external DACs that convert the modulator's multibit output state into an equivalent analog value. Instead of a multibit modulator one can use a 1-bit modulator. Applying a sufficiently high oversampling coefficient OSR (*oversampling ratio*) and using the noise-shaping technique we can achieve high resolution and the required dynamic range of the converter. A single-bit converter based on delta-sigma modulator may be easily implemented in digital circuits because it operates on two states only : "0" and "1".

The idea of delta-sigma modulator operation relies on appropriate modification of the modulator's transfer function for noise in such a way that the noise energy within the used frequency band is minimized. This process is known as noise shaping. Shaping functions of higher orders can be achieved using parallel or MASH architectures of converters.

The delta-sigma modulator can be used for quantization of signals which may be continuous in time as well as discrete in time. Separation of the signal from noise in a digital-to-analog converter is achieved by using a simple analog filter. Delta-sigma converters require filters with less rigorous characteristic because the sampling frequency of the signal is much higher than the Nyquist frequency [7]. Hence, the filter passband may be much wider [7]. Detailed requirements for RC filters used for analog signal reconstruction for delta-sigma digital-to-analog converters can be found in [5]. Figure 1 shows a classical model of a delta-sigma first-order modulator presented in many papers [2, 8, 9].

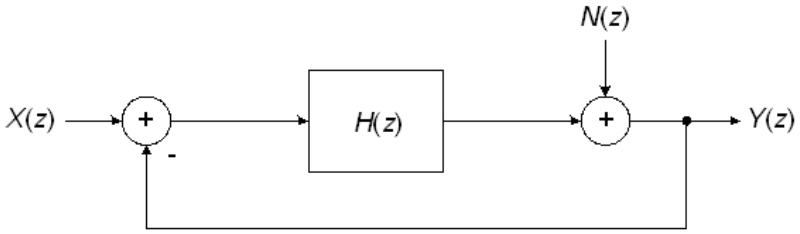

Fig. 1. Theoretical model of delta-sigma modulator.

The output signal $Y(z)$ is the sum of input signal $X(z)$ transferred by the system and the noise signal $N(z)$. If we distribute the transfer function $H(z)$ of the modulator into the noise transfer function $H_n(z)$ and signal transfer function $H_x(z)$, the modulator's operation may be described as:

$$Y(z) = H_x(z)X(z) + H_n(z)N(z). \tag{1}$$

Assuming that $H(z)$ function is realized by digital integrator [1], we can easily derive equations for signal and noise transfer functions:

$$H_x(z) = \frac{\frac{z^{-1}}{1-z^{-1}}}{1 + \frac{z^{-1}}{1-z^{-1}}} = z^{-1}, \tag{2}$$

$$H_n(z) = \frac{1}{1 + \frac{z^{-1}}{1-z^{-1}}} = 1 - z^{-1}. \tag{3}$$

From (1)–(3) it follows that the signal is transmitted without change in the frequency domain and is delayed in the time domain only. In first-order modulators the noise is filtered by a first-order high pass filter (at 20 dB/decade). By increasing the order of the modulator one can obtain better attenuation of quantization noise at low frequencies. It should be noted that first-order modulators implemented in FPGA devices have relatively low SNR ratio, because it is directly limited by the maximum operating frequency of the programmable device. Another important drawback of first-order modulators is also the occurrence of limit cycles [4, 10, 11, 12] in the form of output artifacts observed within the useful signal band. In practice, the oversampling ratio OSR is calculated by a well-known formula, as a quotient of sampling frequency f_S and maximum signal frequency f_{BW} multiplied by two:

$$OSR = \frac{f_s}{2f_{BW}}. \tag{4}$$

In the case of first-order modulators each doubling of the OSR causes an increase of SNR by 9 dB, which corresponds to an increase of resolution by 1.5 bit.

Second-order modulators guarantee much better properties of noise shaping. We can certainly use modulators of order higher than two for further improvement, but we must remember that they are unstable in some conditions. Examples of third- and fifth-order digital-to-analog converters are described in [1]. In second-order modulators each doubling of the OSR results in an increase of SNR by 15 dB or in an equivalent increase of the resolution by 2.5 bit. The SNR ratio of a second-order modulator [8] is related to the OSR according to the Eq. (3):

$$SNR = \frac{\pi^2}{\sqrt{60}}(OSR)^{-\frac{5}{2}}. \tag{5}$$

Equation (8) is correct for sinusoidal signals and under the assumption that the sampling frequency is much higher than the signal bandwidth.

The parameters of a delta-sigma modulator can be improved if we quantize the modulator's quantization noise in a second modulator and add the result to the output

of the first modulator in order to reduce its own quantization noise. Architectures of this type are known as cascaded modulators or MASH [2]. Figure 2 shows a simple cascaded modulator containing two first-order delta-sigma modulators [13].

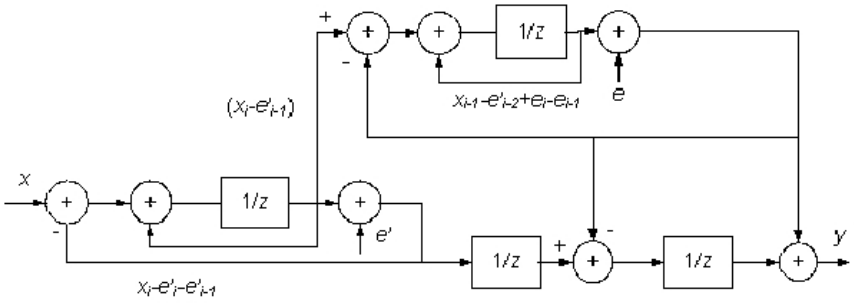

Fig. 2. Cascaded delta-sigma modulator built out of two first order modulators.

As we can see, the output of the integrator in the first modulator is connected to the output of the second modulator. In Figure 2 the symbol *e*' denotes the first modulator's quantization error, and the symbol *e* is the second modulator's quantization error. The output signal may be calculated as:

$$y_i = x_{i-2} + e'_{i-2} - e'_{i-3} + e_i - 2e_{i-1} + e_{i-2}. \tag{6}$$

3. VIRTEX-4 FAMILY AS A PLATFORM FOR IMPLEMENTATION OF DELTA-SIGMA MODULATORS

The Virtex-4 family of programmable devices is a modern generation of Xilinx's FPGA devices [14]. They are fabricated using 90 nm technology which accelerates operation and decreases power consumption. The Virtex-4 family consists of three platforms: LX, FX and SX. Main differences between these platforms result from different internal architectures. The basic LX family is dedicated to highly-efficient logic systems. Each family offers devices of different capacities and resources. In our project we used the XC4VLX25 device that has enough logic resources for implementation of any delta-sigma DAC architecture considered in this paper. Even the most complex structures of DAC examined in our laboratory do not use more than a few percent of the device's resources and just one output pin.

An important feature of the Virtex-4 family are built-in clock generation blocks DCM (*digital clock manager*) that helped us testing DACs in a wide range of frequencies using a single external 100 MHz clock. The XC4VLX25 device includes eight DCMs and additional four clock dividers. Each DCM may be used for clock signal distribution, delay compensation, frequency synthesis and phase shifting by 90°,

180° and 270°. The DCM block set is useful for digital system designers and eliminates external PLL loops. Built-in BRAM (Block RAM) memory with a capacity of 1296 kb has been used in our project as a sinus function look-up-table for test signal generation, and also as a memory holding samples of the DAC's output signal (10^4B).

Programmable devices, due to their high speed and flexible architecture, are an interesting alternative to ASIC devices and signal processors in digital signal processing [15, 16, 17]. Nowadays, advanced digital systems contain, apart from the DSP processor, an additional FPGA chip for fast signal processing. Most DSP operations need many multiplication and accumulation operations, thus modern programmable devices have built-in hardware multiply and accumulation blocks (MACs). In this way a single FPGA chip can perform many parallel DSP operations. Some Virtex-4 devices contain even 512 MACs. Each of them consists of a dedicated 18-bit multiplier, adder and 48-bit register.

Programmable logic offers flexibility of DSP devices at higher speed, capacity and lower cost. In some applications programmable devices replace DSP devices completely, in others they co-operate with DSP processors relieving them of some computing. For example most of DSP processors can execute a single multiplication and accumulation operation in a single machine cycle, while programmable devices like the XC4VSX54 are able to execute 512 multiplications and accumulations simultaneously with a 500 MHz clock.

4. EXPERIMENTAL RESULTS

Experimental tests of DACs have been performed using an evaluation board ML401 from *Xilinx* with the XC4VLX25FF668 device. Figure 3 shows a simplified block diagram of our test-bed.

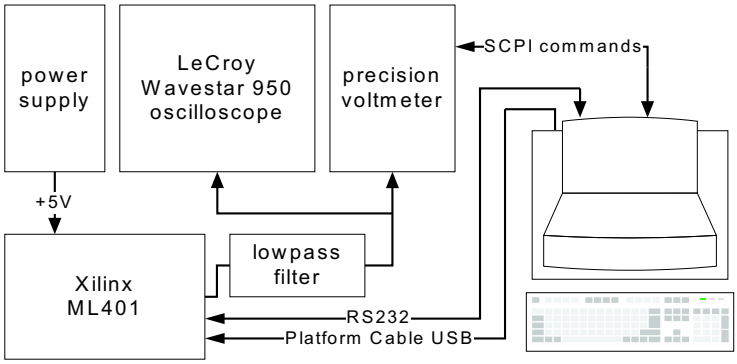

Fig. 3. Block diagram of test-bed.

To compare different versions of DACs we have assembled a digital measurement system that automated measurement sessions by using additional blocks programmed in the device and appropriate MATLAB scripts. The functional diagram of the test-bed is presented in Fig. 4. An oscilloscope featuring a wide measurement band has been used to observe the output signal from the DAC, to measure dynamic parameters and to obtain the output spectrum. Simultaneously, we calculated the output spectrum using a PC and relevant software. In order to do this, the sequence of samples registered in the internal BRAM via RS232 interface was analyzed by an appropriate MATLAB script that calculated and plotted the frequency spectrum. Calculations are based on a standard procedure using Hanning's window.

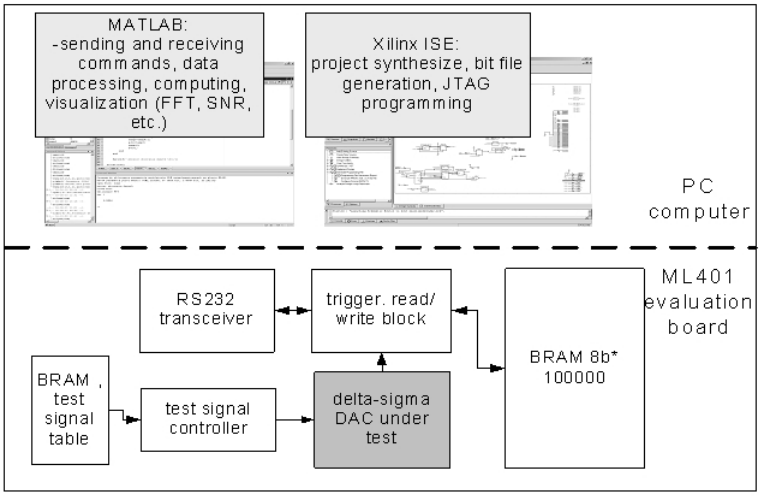

Fig. 4. Functional diagram of test-bed.

Differential nonlinearity has been determined by measurements of DAC's output voltage (after low-pass filtering in a simple RC filter) using a precision voltmeter Agilent 34401A [20]. The sequence of digital readouts from the voltmeter was transmitted via RS232 to the PC and then analyzed in a MATLAB environment. According to the remarks published in [5], the time constant of the RC filter has been chosen using the criterion of minimum output signal pulsations. In our case R = 3.3 kΩ and C = 4.7 nF. For each digital input code the output voltage has been measured 50 times and its mean value has been used as a final estimate of the DAC's output signal. This procedure has been repeated within the full measurement range, i.e. for input codes from 0 to 2^{16}. Since the complete test was time-consuming, all measurements have been fully automated. The precision voltmeter was controlled by SCPI (*Standard Commands for Programmable Instruments*) command language sent through RS232

from the MATLAB environment. Due to the high oversampling ratio and modulator's order not greater than two, a simple RC filter can be applied.

Following the method of DAC's testing described in [1] we used a sinusoidal signal and a constant signal generated by the counter. All necessary test blocks, except the test signal generator, are embedded in the programmable device which also includes a bidirectional unit for RS232 communication and readout circuits of DAC's output signal. To analyze measurement results a number of scripts have been written in MATLAB environment that automated the measurement process and can be easily modified to perform different measurement sessions.

To describe the behaviour of tested DACs we used power spectrum diagrams obtained with the Hanning windowing function which reduces spectrum leakage. The FFT spectrum transform has been calculated using $2^{19} = 524288$ signal samples. At the sampling frequency $f_s = 100$ MHz, the frequency resolution of FFT is equal to 190.734 Hz. Each spectrum diagram is described by the value of SFDR coefficient related to the input signal and expressed in decibels [dBc]. SFDR is defined as the ratio of the RMS value of the input signal to the peak spurious signal at the output. In this method of SFDR determination the use of an analog filter is not necessary. Therefore, the spectrum is obtained by the FFT transform of the original signal at the DAC's output. However, due to oversampling, the number of samples used by FFT is very large.

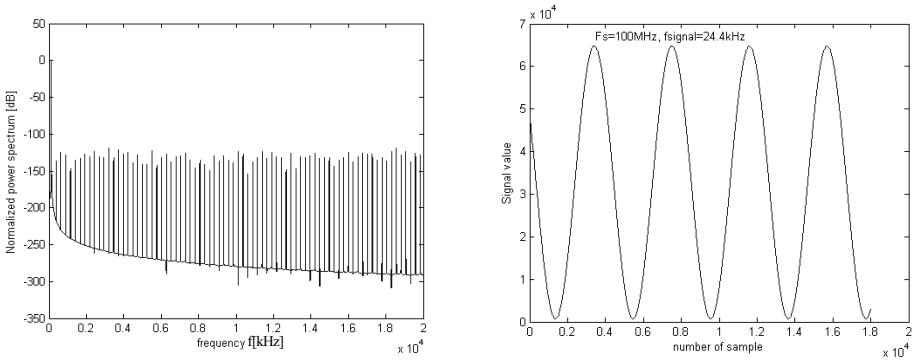

Fig. 5. Spectrum and time diagram of test signal.

Obviously, the form of the test signal used for DAC measurement impacts on the measurement results. In our tests we used a sinusoidal signal table. Before the measurement session the test signal is analyzed by FFT in MATLAB and identical conditions are used for generation and implementation of the test signal within the system. The main measurement results are presented in Fig. 5. The noise floor is about −260 dB, however one can observe that the spectrum bins at higher harmonic frequencies are about the −125 dB level. This phenomenon is partly caused by an

arithmetic which in our case uses 16-bit resolution, and by lowering of the mean noise level due to the large sample size of FFT (processing gain).

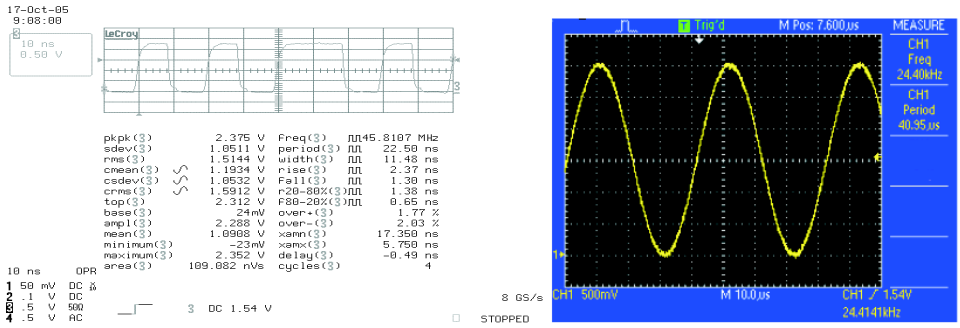

Fig. 6. Delta-sigma modulator's output at programmable device pin and signal at the output of low-pass RC filter.

The measurement method described above is very accurate but it does not take into account the influence of output parameters on converter's parameters. The speed of programmable device output buffers, output capacity, voltage levels for logical "1" and "0", output current efficiency have significant impact on measurement results. Fig. 6 presents a sample oscillogram of the output signal from delta-sigma modulator for LVTTL output type before the RC filter and after filtering (R = 3.3 kΩ, C = 1 nF).

Our tests of DACs have been performed using 16-bit resolution. Maximum converter's voltage output value FS (full scale) depends on FPGA output type. To achieve the best current efficiency the TTL output type was chosen for converters, which gives the output voltage range from 0 do 3.3V for XCV4LX25 device. Thus, the smallest increase of the converter's output voltage is equal to 50.35 µV.

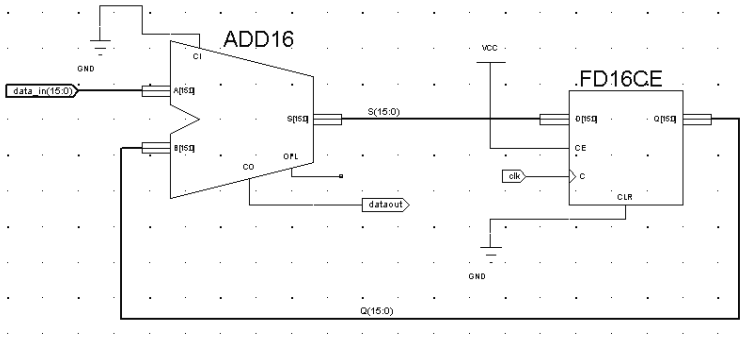

Fig. 7. Implementation of simple first order digital-to-analog converter.

The simplest digital-to-analog converter can be built using an adder with carry output and flip-flop [8, 18]. Figure 7 shows a diagram of a 16-bit input word converter. Carry output from adder is converter's output. The presented architecture can also be implemented in the DSP block in Virtex-4 device. A detailed description of the FPGA implementation of all presented architectures as well as the measurement system configuration are available on-line from the author's web page [21].

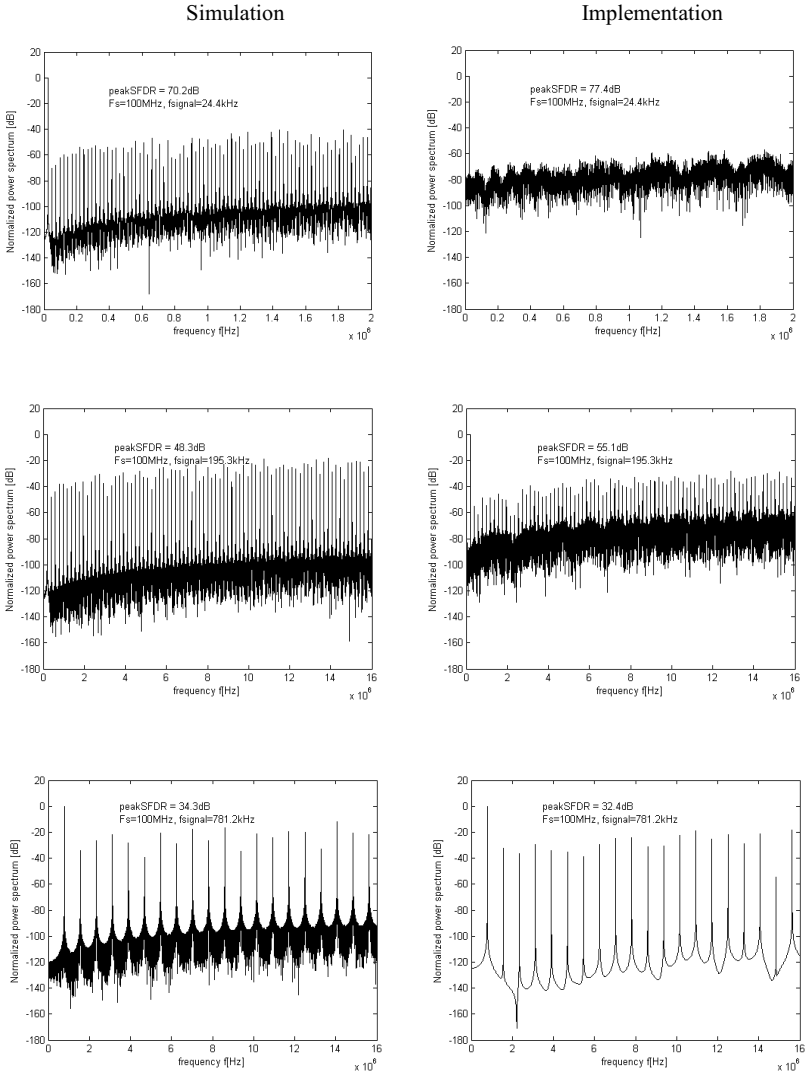

Fig. 8. Power spectrum of first order delta-sigma modulator, first type architecture from Fig. 7.

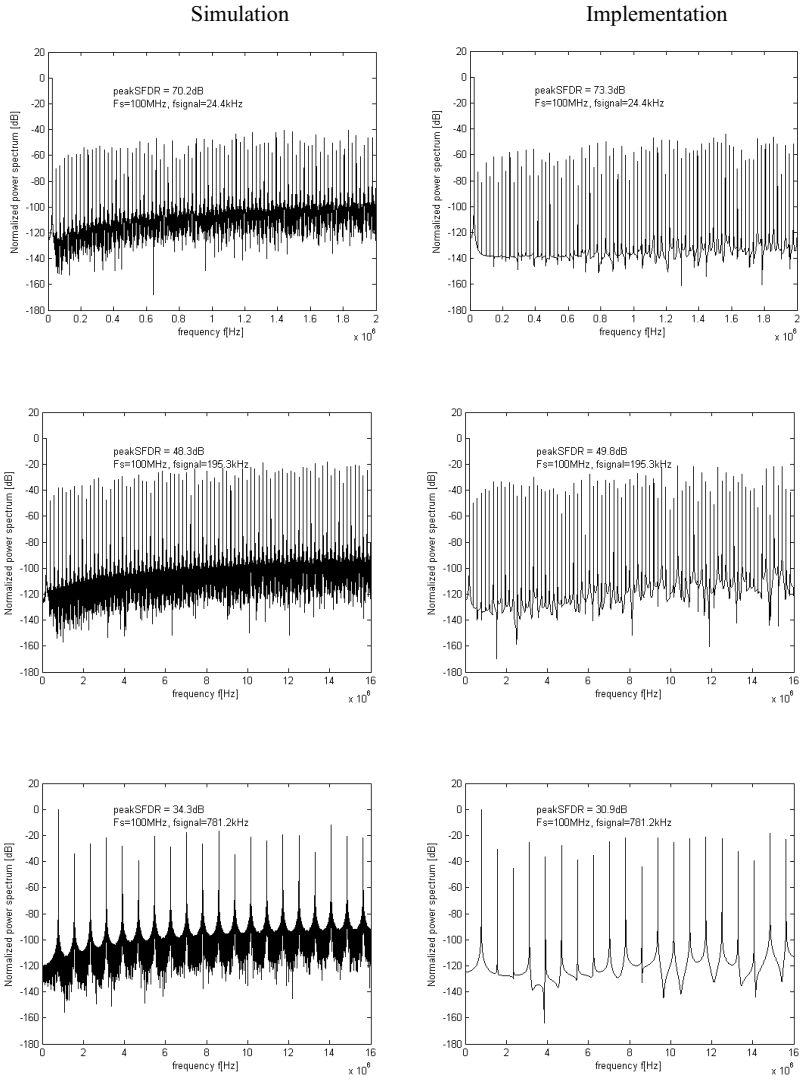

Fig. 9. Power spectrum of first order delta-sigma modulator, architecture from Fig. 1.

Experimental tests of implemented DACs show that this architecture uses very few logical resources while its maximum operating frequency approaches 330 MHz. Figure 8 shows a part of the power spectrum of the converter's output signal obtained by applying to the input a sinusoidal test signal at three frequencies f_s = 24.4 kHz, f_s = 195.34 kHz, f_s = 781.2 kHz and at a sampling frequency F_s = 100 MHz. We also performed a simulation in identical conditions as for hardware implementation. The greatest SFDR is equal to 70.2 dB at the signal frequency f_s = 24.4 kHz. It should be noted that experimental results for f_s = 24.4 kHz, f_s = 195.34 kHz differ slightly from simulation results. An increased noise level and decreased harmonics level may be the result of metastability, which inserts additional dither used in digital-to-analog and analog-to-digital converters for parameter improvement. Figure 9 presents measurement results for a first-order delta-sigma modulator with the architecture presented in Fig. 1 [5]. The modulator's block was coded in VHDL language. Since the architecture of the modulator is of first-order type, the results of simulations are identical as for the previous modulator. In this case all experimental results are identical as in the simulation.

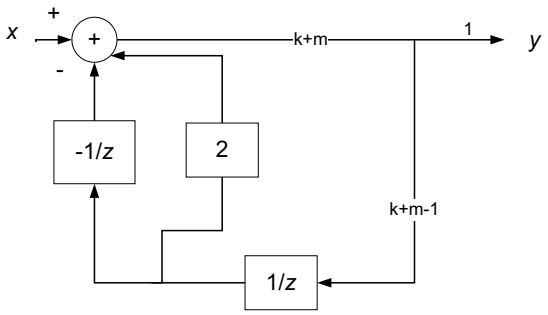

Fig. 10. Second order delta-sigma modulator with error feedback architecture.

Figure 10 shows the architecture of a second-order converter described in [2], which has been tested using our test-bed.

The noise floor for the second-order modulator described by the architecture shown in Fig. 10 is the smallest one. Experimental results are presented in Fig. 11. As previously, modulators harmonic bins are visible. Maximum SFDR for f_s = 24.4 kHz is 74.2 dB.

To estimate the linearity of DACs, the differential nonlinearity functions (DNL) have been calculated and plotted for three types of modulators. A constant 16-bit value has been applied at the input. The output values were measured for all input codes by a precision meter which was controlled from the MATLAB application. According to theory, the linearity of first-order DACs is rather poor and the maximum DNL is equal to +0.36/−0.2% FS. The linearity of the second-order DACs is much better – the maximum DNL is equal to ±0.02% FS.

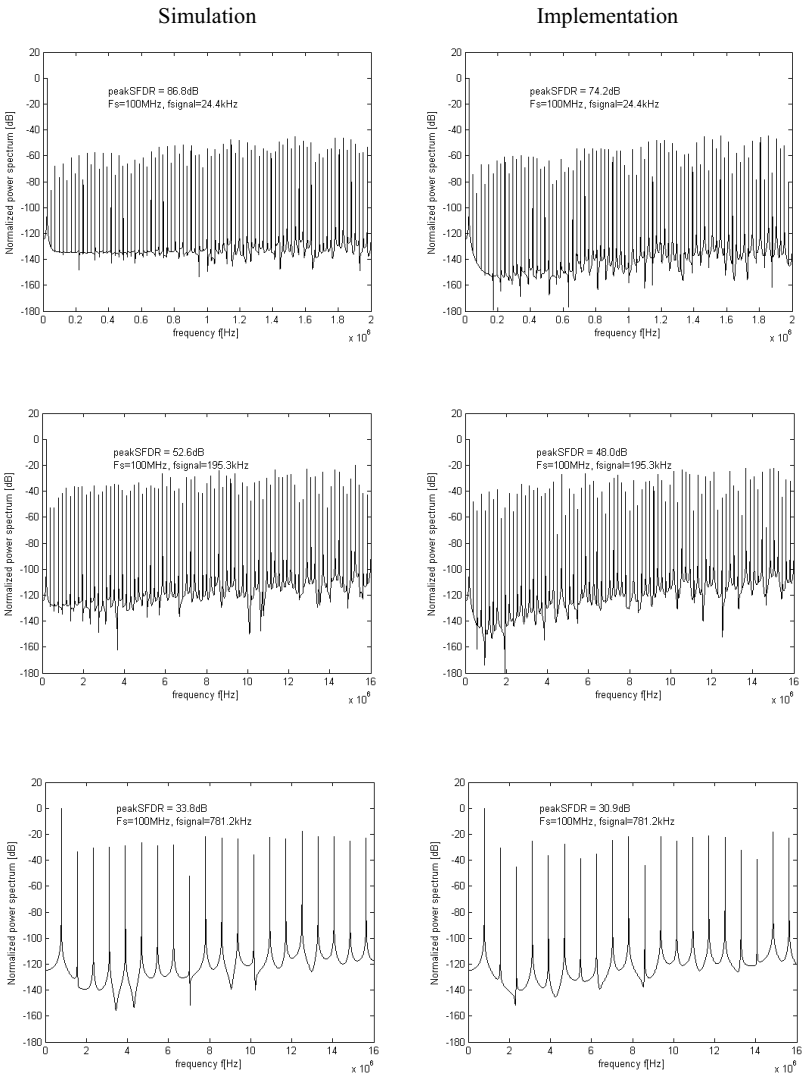

Fig. 11. Power spectrum of second order modulator, architecture from Fig. 10.

Figure 12c shows the action of simple correction of the DNL error. To do this an additional comparator/corrector is used. The output codes visible as peaks (artifacts) are replaced by neighbouring codes. In this way some output values are missed, but the resulting DNL can be lowered significantly. This method is especially efficient for DC and low frequency signals.

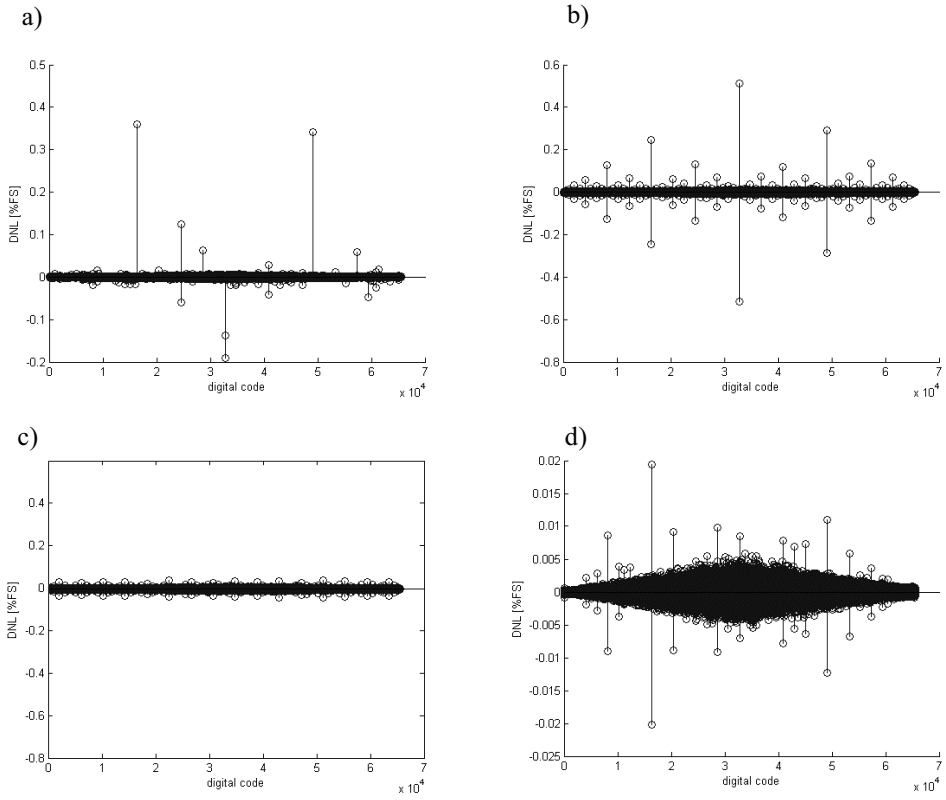

Fig. 12. Differential linearity DNL of three architectures of modulators: a) first order modulator from Fig. 7, b) first order modulator from Fig. 1, c) first order modulator from Fig. 1 after correction, d) second order modulator from Fig. 10.

An important limitation of delta-sigma modulation used in DACs described above is their maximum operating frequency and resulting quantization error. To reduce this error a well known dithering method can be used. We tested this method by simulation in MATLAB environment. The linear feedback shift register (LFSR) may be used for random signal generation. A sample design of such a register with 168-bit period which utilizes very few resources of the programmable device is described in [19]. An interesting property of the DNL function obtained in this case is its symmetry for some input codes. This symmetry is caused by register's overflow at frequencies related

to the input signal. Applying the dithering method again we can reduce these errors significantly. Further improvement of the DNL may be also obtained by a double RC filter.

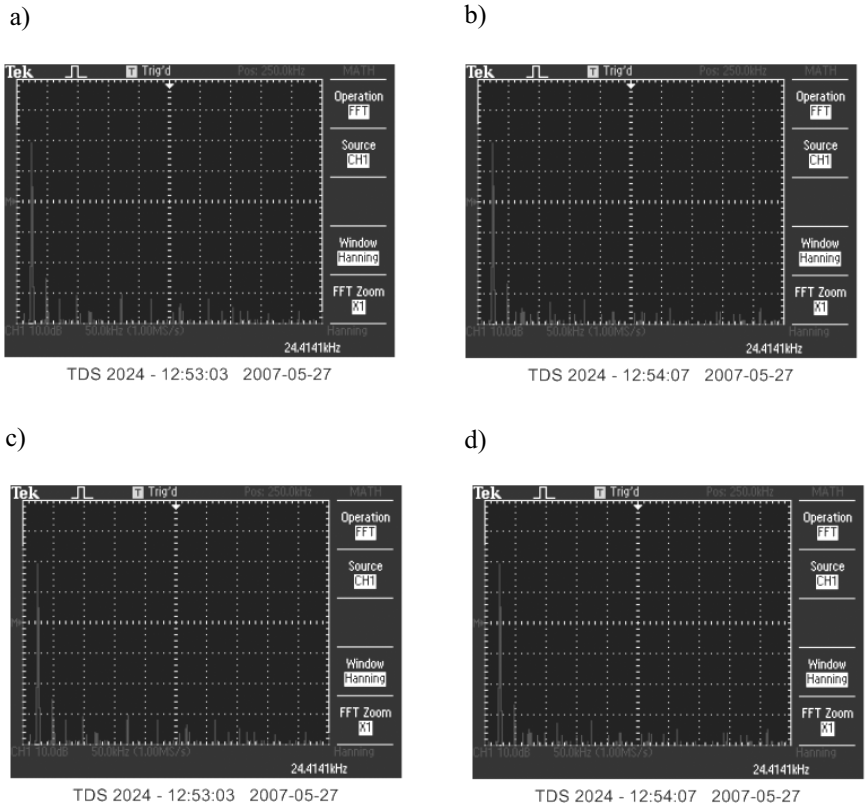

Fig. 13. Effects of differential linearity DNL in output spectrum of three architectures of modulators: a) first-order modulator from Fig. 7, b) first-order modulator from Fig. 1, c) second-order modulator from Fig. 10, d) spectrum of the reference signal from generator AFG 3021.

Figure 13 shows the output spectrum of a 24.4 kHz sinusoidal signal generated by different DAC architectures at the clock frequency equal to 100 MHz. It should be noted that in each case the level of the first harmonic is similar, while the lowest level of high order harmonics may be observed for the second-order architecture. The output signal from DACs has been filtered using a RC lowpass filter (R = 3.3 kΩ, C = 1 nF). As a reference we used a sinusoidal signal generated by the Tektronix AFG 3021 signal generator (Fig. 13d). It can be seen that plots of the DAC's output spectrum do not significantly differ from the reference spectrum.

Figure 14 shows a comparison of resources used and the maximum operating frequencies for different DAC's versions described in this paper. The values of frequencies given in Fig. 14a are obtained by a time analyzer from the *Xilnix* ISE environment.

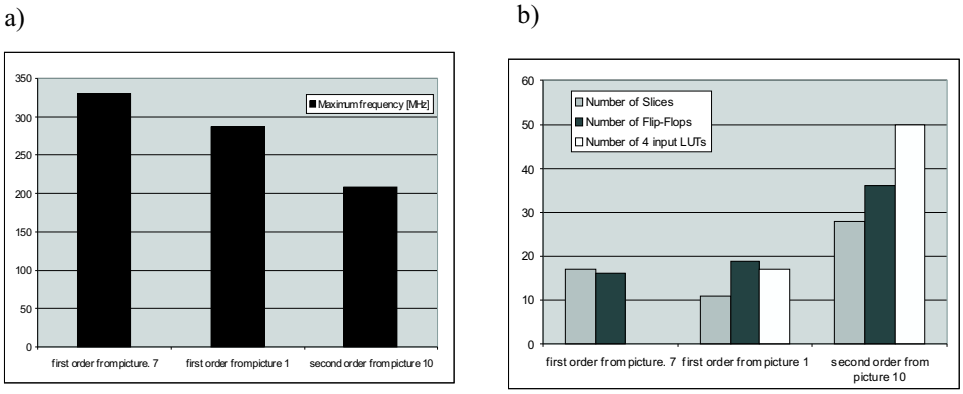

Fig. 14. a) Maximum operating frequencies and b) used resources for different types of converters.

We also tested the converter's response to a step change of input data from 0 to 0.95 of full scale. The rise time measured by the oscilloscope was similar for all architectures and equals 46 μs, while the output settling time was equal to 112 μs. We did not observe glitch pulses or other artifacts. The measurements were performed at the clock frequency of 100 MHz and with a RC filter: R = 5.1 kΩ, C = 4.7 nF. Rise time was measured as the time required for the signal to change from 10 to 90% of the maximum output value. Settling time was measured from the change of the input digital code to the time when the output comes within the error band of 1 LSB.

Obviously, the dynamic parameters of the DAC depend on the clock frequency and RC filter transfer function. One can improve the dynamic behavior of the DAC by appropriate tuning of the RC time constant, but at the cost of an increase of output noise level. By decreasing the time constant we get a corresponding reduction of rise time at the DAC output but also lower resolution. For example, with R = 3.3 kΩ and C = 4.7 nF we obtained a rise time equal to 38 μs and settling time equal to 82 μs, while with R = 2.7 kΩ and C = 100 pF the rise time was reduced to 1.0 μs and settling time equals 2.5 μs.

Figure 15 shows the theoretical maximum SNR plotted as a function of the order L of ideal delta-sigma DAC and oversampling ratio OSR. Designers can use these plots for initial, rough estimation of SNR for different applications. Obviously, for fast and precision conversion we need high-order modulators. However, since the FPGA platform requires 'pure digital' architecture of DAC (single-bit quantizers) in practice designers can choose the oversampling ratio and modulator's architecture.

From Fig. 15 it follows that using a first-order modulator operating at oversampling ratio OSR = 1024 we get the SNR = 86 dB which is equivalent to a resolution of

14 bits. Since the maximum clock frequency for the Virtex-4 FPGA platform is about 300 MHz, the resulting maximum output signal frequency equals 292 kHz. On the other hand, for extremely low band signals, e.g. 100 Hz, the first-order modulator operating at the clock frequency of 100 MHz uses the oversampling ratio OSR = 10^6. It means that the theoretical signal-to-noise ratio SNR_{max} is equal to 176 dB and the equivalent resolution approaches 29 bits. Obviously, in practice these parameters are significantly limited by the noise effects.

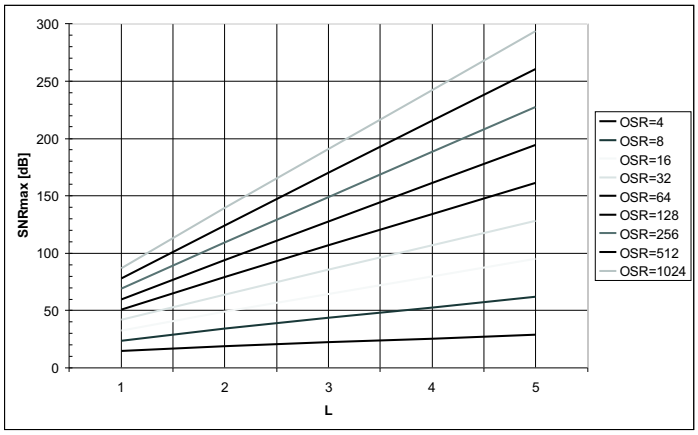

Fig. 15. Plots of the maximum signal-to-noise ratio SNR_{max} for single-bit sigma-delta modulators versus the modulator's order L and oversampling ratio OSR.

Furthermore, the important factor that affects the maximum output frequency is the order L of the modulator. According to the theoretical analysis from Fig. 15, the first-order DAC operating at the 300 MHz clock frequency and OSR = 60 features the maximum output frequency of 5 MHz and 8-bit resolution. At the same conditions the second-order and fourth-order DACs can generate signals up to 17 MHz and 37 MHz, respectively.

5. CONCLUSION

The DAC based on a first-order delta-sigma modulator having an architecture of first type is simple for implementation and uses very few resources (17 macrocells, or 0.07% of XCV4LX25 total resources). Its maximum operating frequency of about 330 MHz is the highest one comparing with the other architectures. A DAC of this type is especially useful for signal processing in a narrow band. In the case of a low-frequency regular input signal this modulator generates significant noise which is typical for first-order modulators. This noise may be avoided by applying high frequency jitter not correlated with the input signal. The second version of the first-order converter has better SNR.

Its maximum operating frequency is about 287 MHz. Implementation of the converter for different resolutions is fast and easy by appropriate modifications of the modulator's VHDL description. The second-order converter has the best SFDR, in accordance with theory. On the other hand, its implementation in FPGA requires more resources and the architecture is more complicated which decreases the maximum operating frequency.

All examined modulators are stable. Further improvement of maximum operating frequencies is possible by careful optimization of timing within the project. For conversion of wide band signals modulators of order higher than two are needed. Good solutions are cascaded converters and interleaved architectures but at the risk of loosing stability. Some useful criteria for choosing the proper architecture of the modulator are given in [8].

To summarize, all presented delta-sigma modulators implemented in FPGA chip perform well, especially for narrow-band signals. According to the theoretical calculations they can operate at the maximum frequency of about 200 MHz and 16-bit resolution. The maximum bandwidth of the signal for first-order converters is equal to 82 kHz and 1.3 MHz for second-order DACs. We confirm their practical usefulness by experimental tests of the SFDR. Of course, as one can expect, the practical accuracy of DACs is limited by noise and low-pass output filtering.

The DACs described in the paper can be used in multichannel systems, because each single converter needs very few resources and only one pin. Further improvements may include linearity correction and noise reduction modules.

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